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# MS-7A70

mATX:243\*226

Ver: 10

## Intel -KabyLake-S plamform

### CPU:

LGA1151  
CPU POWER PAK \*3 Phase  
GT POWER PAK \*2 Phase

### System Chipset:

SPT-H :B250 colay H270

### Onboard Chip:

HD Audio Codec: ALC892  
SIO: NCT6795D  
Flash ROM: SPI 64 MB

### PWM:

VCORE - RT3606  
DDR - RT8125E  
PCH(1.0V) - RT8125E  
VCCSA - RT8125E  
VCCIO - NB681(Converter)  
VPP25 - MP2147

### Main Memory:

DDR4 \* 4 (Dual Channel)

### LDO:

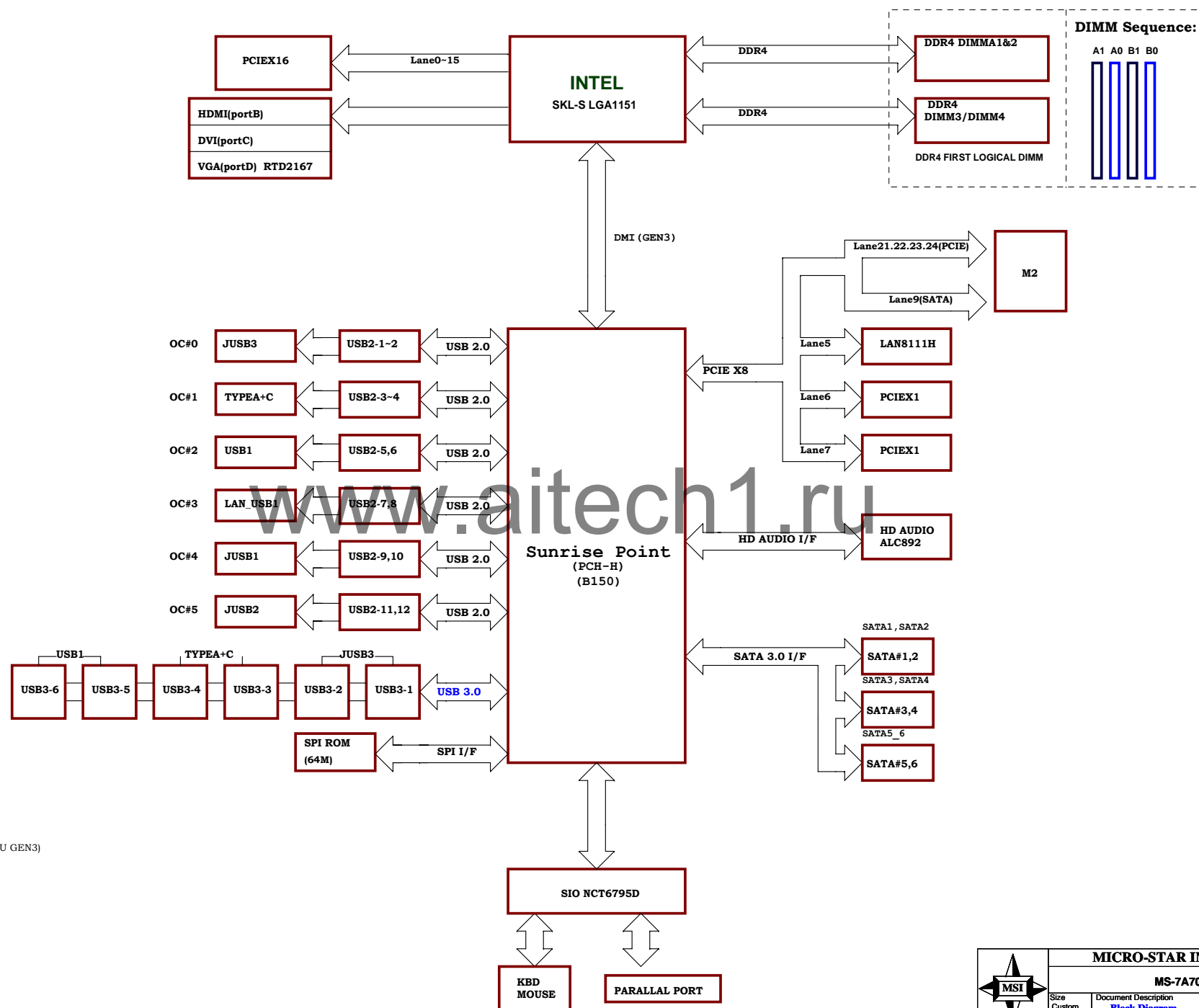
VCCSTPLL - GS7133

### ACPI:

5VDAUL:uP7501  
5VDIMM:uP7501  
3VSB:GS7133+PN MOS  
3VDSW:GS7133

### Expansion Slots:

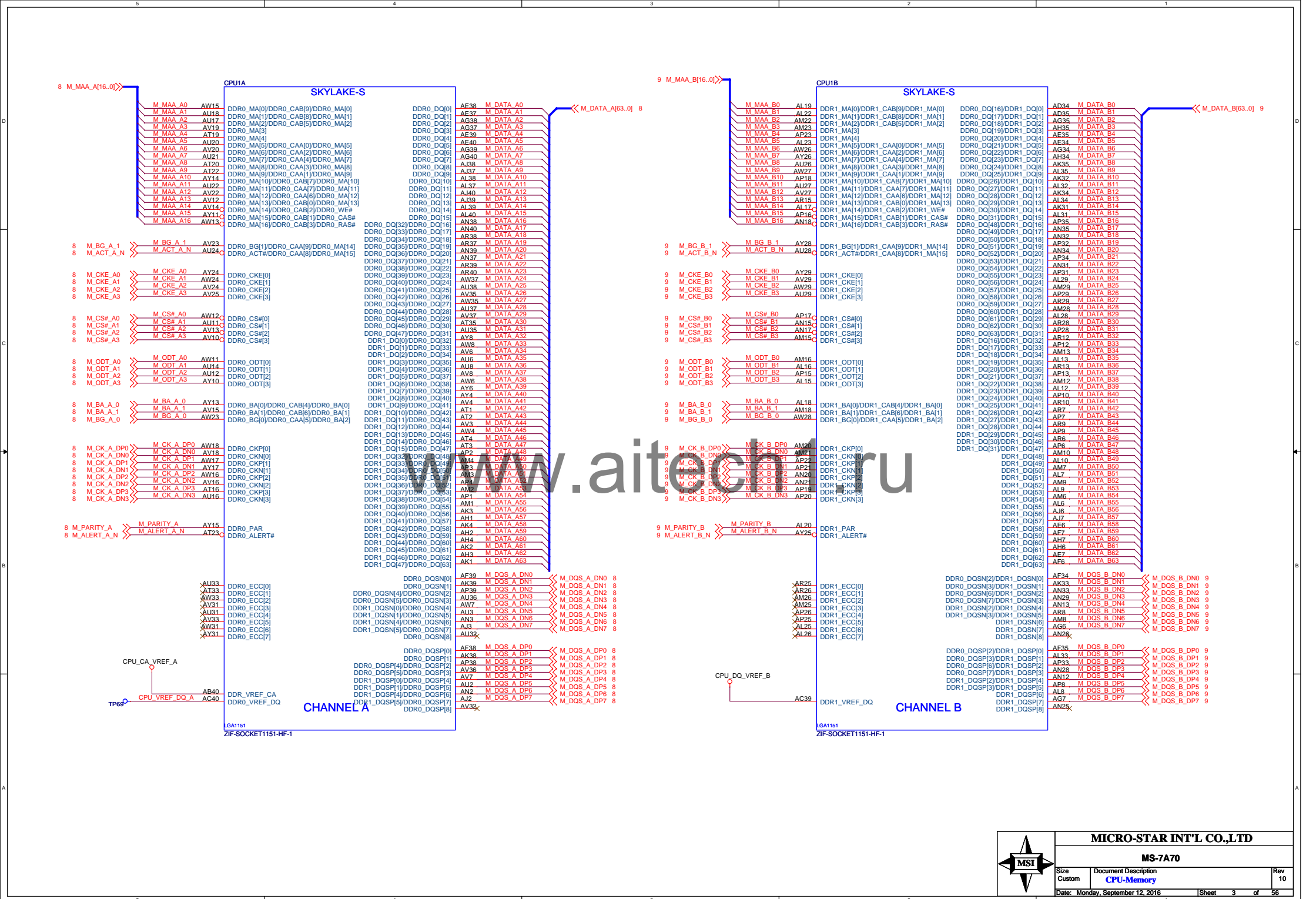
PCI Express (X16) Slot \* 1  
PCI Express (X1 ) Slot \* 2

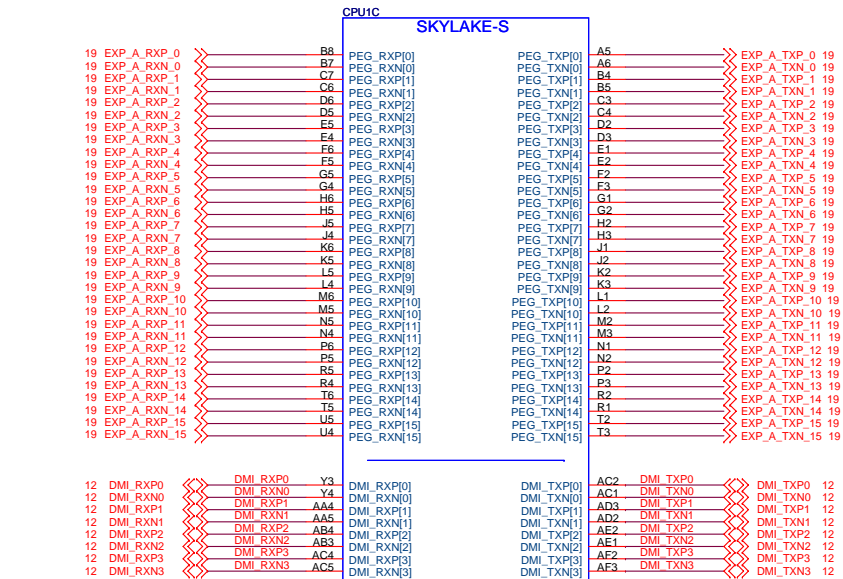
**Slot Sequence:**

**MICRO-STAR INT'L CO.,LTD**

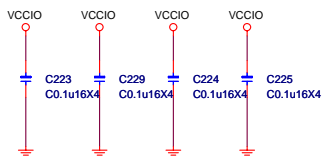
**MS-7A70**

Size Custom	Document Description <b>Block Diagram</b>	Rev 10
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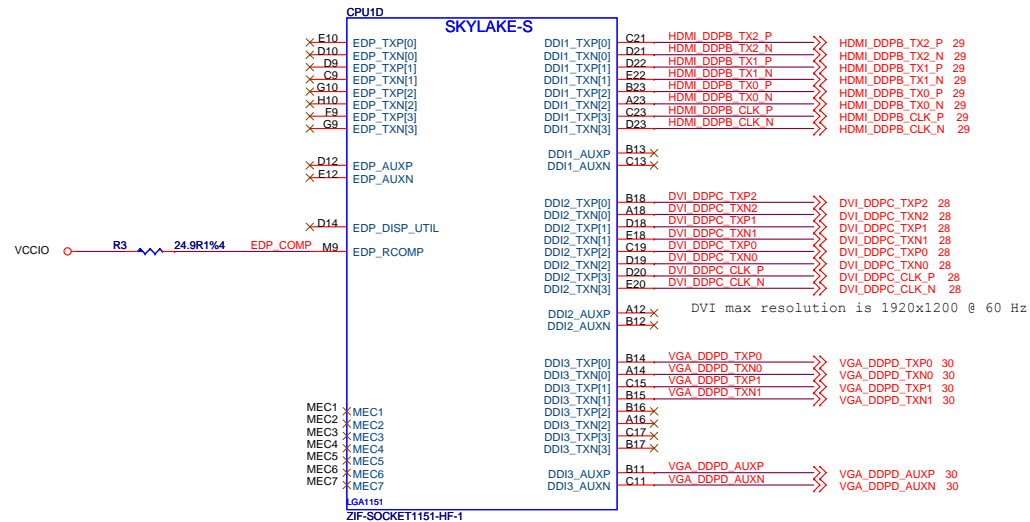
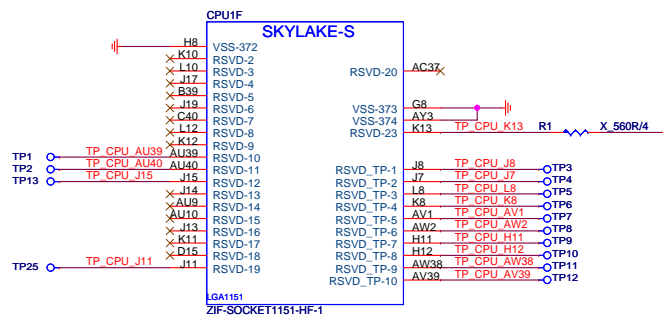




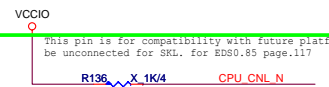
VCCIO R2 24.9R1%4 PEG\_COMP L7 PEG\_RCOMP  
L<=0.4 inch



For DMI reference VCCIO USE  
please close to DMI via side





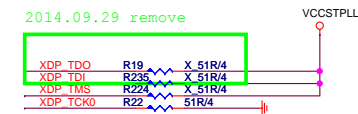
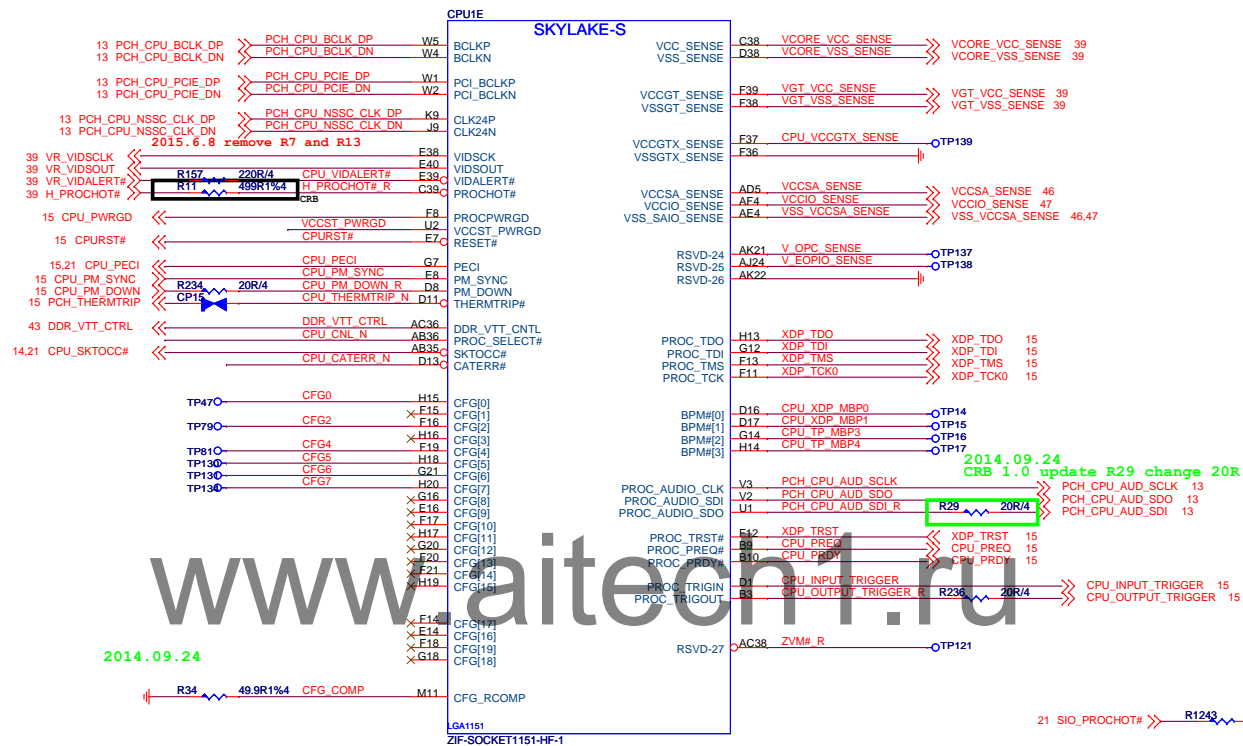


2015.04.23 for debug use



## CFG Table

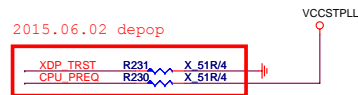
CFG Table			
7	HIGH	LOW	DESCRIPTION
0	NO LOCK	LOCK	PCI PG LOCK
1			RSVD
2	NORM	REVERSE	PG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PGCFGSEL[0]
6	DISABLE	ENABLE	PGCFGSEL[1]
7	RESET#	SIGS REQ	PG CEEB TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



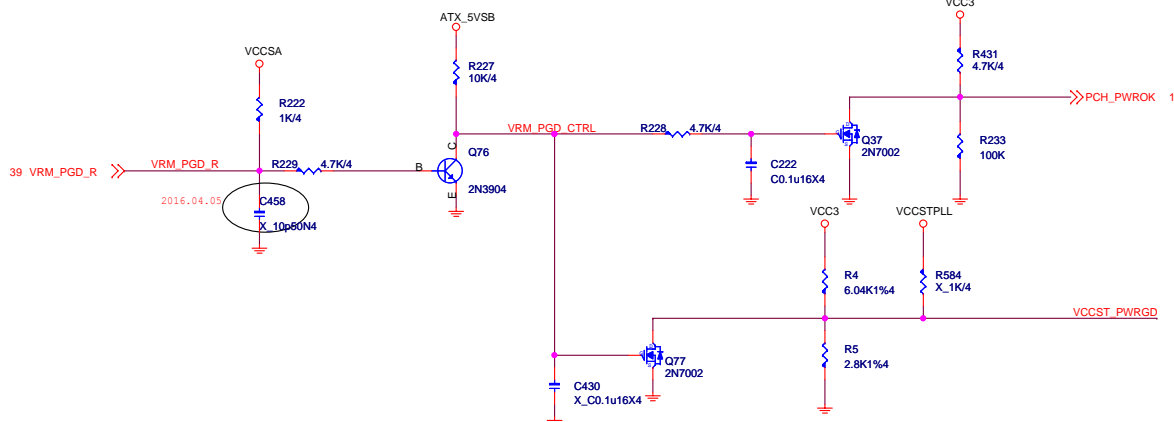
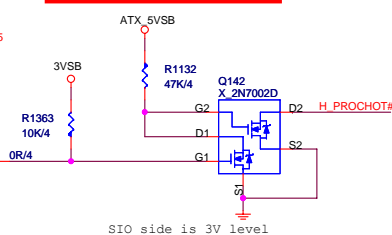
```

Close CPU <1100 mil
1000 mil < CPU XDP MBP0~1 < 6000 mil

```

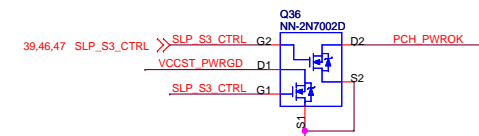


2015.06.02 depop



modify 2014.09.19

POWER DOWN



```
For VCCST_PWRGD deassertion
max:lus
```

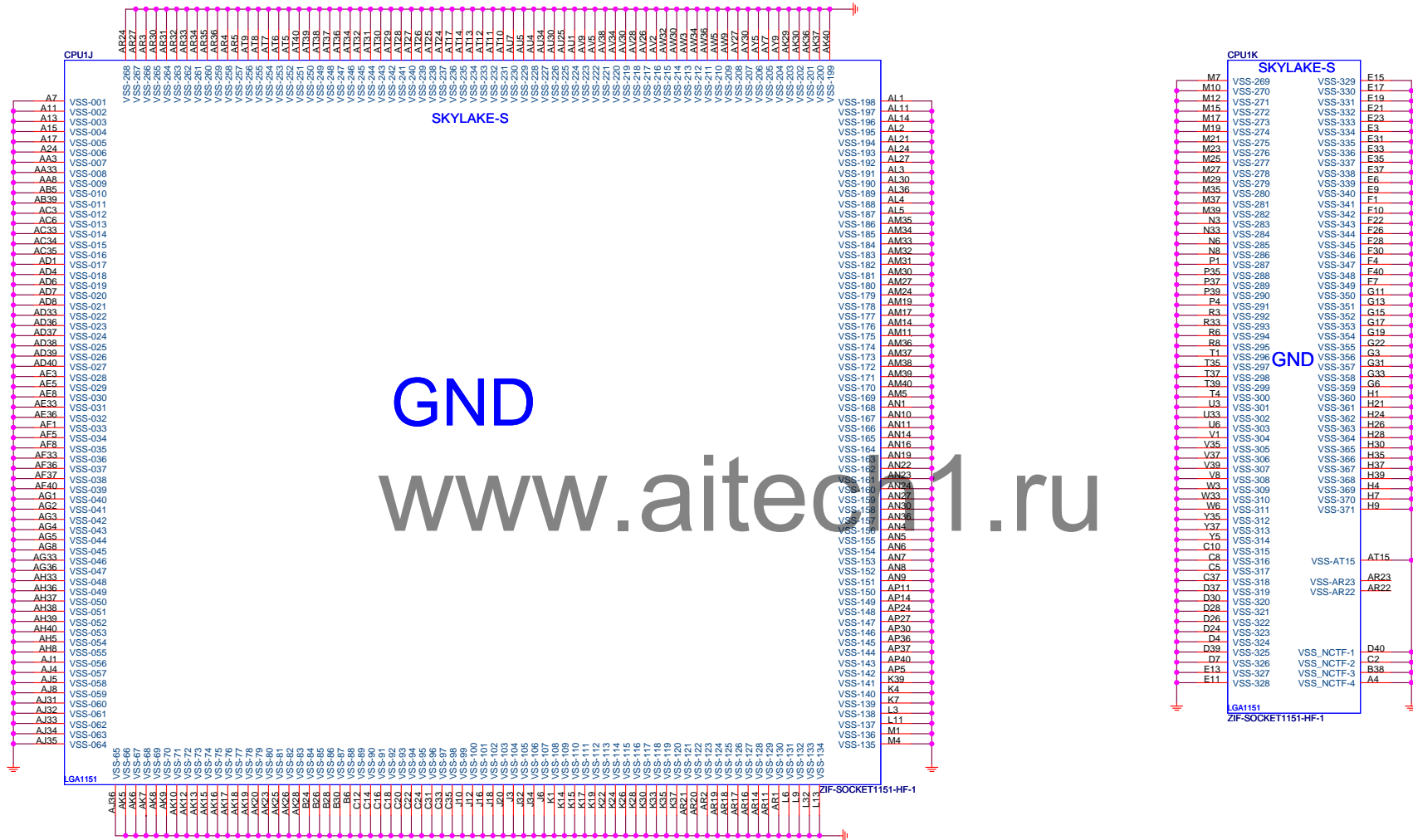


**MICRO-STAR INT'L CO.,LTD**

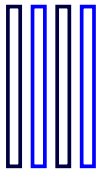
**MS-7A70**

Size Custom	Document Description <b>CPU-Control/MISC/CFG/Audio</b>	Re
Date: Monday, September 12, 2016		Sheet 5 of 56





A1 A0 B1 B0



3 M\_DQS\_A\_DP7 >> M\_DQS\_A\_DP7 278 DQS7P  
3 M\_DQS\_A\_DN7 >> M\_DQS\_A\_DN7 277 DQS7N  
  
3 M\_DQS\_A\_DP6 >> M\_DQS\_A\_DP6 267 DQS6P  
3 M\_DQS\_A\_DN6 >> M\_DQS\_A\_DN6 266 DQS6N  
  
3 M\_DQS\_A\_DP5 >> M\_DQS\_A\_DP5 256 DQS5P  
3 M\_DQS\_A\_DN5 >> M\_DQS\_A\_DN5 255 DQS5N  
  
3 M\_DQS\_A\_DP4 >> M\_DQS\_A\_DP4 245 DQS4P  
3 M\_DQS\_A\_DN4 >> M\_DQS\_A\_DN4 244 DQS4N  
  
3 M\_DQS\_A\_DP3 >> M\_DQS\_A\_DP3 186 DQS3P  
3 M\_DQS\_A\_DN3 >> M\_DQS\_A\_DN3 185 DQS3N  
  
3 M\_DQS\_A\_DP2 >> M\_DQS\_A\_DP2 175 DQS2P  
3 M\_DQS\_A\_DN2 >> M\_DQS\_A\_DN2 174 DQS2N  
  
3 M\_DQS\_A\_DP1 >> M\_DQS\_A\_DP1 164 DQS1P  
3 M\_DQS\_A\_DN1 >> M\_DQS\_A\_DN1 163 DQS1N  
  
3 M\_DQS\_A\_DP0 >> M\_DQS\_A\_DP0 153 DQS0P  
3 M\_DQS\_A\_DN0 >> M\_DQS\_A\_DN0 152 DQS0N  
  
3 M\_CK\_A\_DP1 >> M\_CK\_A\_DP1 218 CK1P  
3 M\_CK\_A\_DN1 >> M\_CK\_A\_DN1 219 CK1N  
  
3 M\_CK\_A\_DP0 >> M\_CK\_A\_DP0 74 CK0P  
3 M\_CK\_A\_DN0 >> M\_CK\_A\_DN0 75 CK0N

235 C2  
237 S3\_N\_C1  
93 S2\_N\_C0  
  
3 M\_CS#\_A1 >> S1\_N 89  
3 M\_CS#\_A0 >> S0\_N 84  
  
3 M\_CKE\_A1 >> CKE1 203  
3 M\_CKE\_A0 >> CKE0 60  
  
3 M\_ODT\_A1 >> ODT-1 91  
3 M\_ODT\_A0 >> ODT-0 87

DIMM\_RESET# 58 RESET\_N  
DIMM1\_EVENT 78 EVENT\_N  
  
3 M\_ALERT\_A\_N >> M\_ALERT\_A\_N 208 ALERT\_N  
3 M\_ACT\_A\_N >> M\_ACT\_A\_N 62 ACT\_N  
3 M\_PARITY\_A >> M\_PARITY\_A 222 PAR

230 SAVE\_N\_NC  
144 RFU-0  
205 RFU-1  
227 RFU-2

DDRIV-288P\_SNOW\_WHITE-RH

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

230 SAVE\_N\_NC  
144 RFU-0  
205 RFU-1  
227 RFU-2

DDRIV-288P\_BLACK-RH-23

DIMM1 (CHANNEL-A)  
ADDRESS = 0:1 [SA1:SA0]

DDRIV-288P\_BLACK-RH-23

DDRIV-288P\_BLACK-RH-23

15.30 SMBCLK\_VCC >> SMBCLK\_VCC R612 OR/4 SMB\_CLK\_DIMM >> SMB\_CLK\_DIMM 9  
15.30 SMBDATA\_VCC >> SMBDATA\_VCC R614 OR/4 SMB\_DATA\_DIMM >> SMB\_DATA\_DIMM 9

DQ-63 280 M\_DATA\_A57  
DQ-62 136 M\_DATA\_A59  
DQ-61 273 M\_DATA\_A61  
DQ-60 128 M\_DATA\_A56  
DQ-59 282 M\_DATA\_A60  
DQ-58 137 M\_DATA\_A62  
DQ-57 275 M\_DATA\_A58  
DQ-56 130 M\_DATA\_A63  
DQ-55 269 M\_DATA\_A55  
DQ-54 124 M\_DATA\_A53  
DQ-53 262 M\_DATA\_A48  
DQ-52 117 M\_DATA\_A50  
DQ-51 271 M\_DATA\_A49  
DQ-50 126 M\_DATA\_A51  
DQ-49 264 M\_DATA\_A52  
DQ-48 119 M\_DATA\_A54  
DQ-47 258 M\_DATA\_A42  
DQ-46 113 M\_DATA\_A46  
DQ-45 261 M\_DATA\_A40  
DQ-44 108 M\_DATA\_A41  
DQ-43 260 M\_DATA\_A43  
DQ-42 115 M\_DATA\_A47  
DQ-41 253 M\_DATA\_A44  
DQ-40 108 M\_DATA\_A45  
DQ-39 247 M\_DATA\_A39  
DQ-38 102 M\_DATA\_A38  
DQ-37 240 M\_DATA\_A37  
DQ-36 96 M\_DATA\_A36  
DQ-35 249 M\_DATA\_A35  
DQ-34 104 M\_DATA\_A34  
DQ-33 242 M\_DATA\_A33  
DQ-32 97 M\_DATA\_A32  
DQ-31 188 M\_DATA\_A27  
DQ-30 43 M\_DATA\_A30  
DQ-29 181 M\_DATA\_A25  
DQ-28 36 M\_DATA\_A28  
DQ-27 190 M\_DATA\_A31  
DQ-26 45 M\_DATA\_A26  
DQ-25 183 M\_DATA\_A24  
DQ-24 38 M\_DATA\_A29  
DQ-23 177 M\_DATA\_A23  
DQ-22 32 M\_DATA\_A19  
DQ-21 170 M\_DATA\_A20  
DQ-20 25 M\_DATA\_A21  
DQ-19 179 M\_DATA\_A18  
DQ-18 34 M\_DATA\_A22  
DQ-17 172 M\_DATA\_A16  
DQ-16 27 M\_DATA\_A17  
DQ-15 166 M\_DATA\_A15  
DQ-14 21 M\_DATA\_A11  
DQ-13 159 M\_DATA\_A8  
DQ-12 14 M\_DATA\_A9  
DQ-11 168 M\_DATA\_A14  
DQ-10 23 M\_DATA\_A10  
DQ-9 161 M\_DATA\_A13  
DQ-8 16 M\_DATA\_A12  
DQ-7 155 M\_DATA\_A7  
DQ-6 10 M\_DATA\_A3  
DQ-5 148 M\_DATA\_A4  
DQ-4 3 M\_DATA\_A1  
DQ-3 157 M\_DATA\_A2  
DQ-2 12 M\_DATA\_A6  
DQ-1 150 M\_DATA\_A0  
DQ-0 5 M\_DATA\_A5

BG-1 207 M\_BG\_A\_1  
BG-0 63 M\_BG\_A\_0

BA-1 224 M\_BA\_A\_1  
BA-0 81 M\_BA\_A\_0

A16\_RAS\_N  
A15\_CAS\_N  
A14\_WE\_N

A17 234 M\_MAA\_A16  
A12 86 M\_MAA\_A15  
A11 228 M\_MAA\_A14  
A10 232 M\_MAA\_A13  
A9 65 M\_MAA\_A12  
A8 210 M\_MAA\_A11  
A7 225 M\_MAA\_A10  
A6 68 M\_MAA\_A9  
A5 68 M\_MAA\_A8  
A4 211 M\_MAA\_A7  
A3 69 M\_MAA\_A6  
A2 213 M\_MAA\_A5  
A1 71 M\_MAA\_A4  
A0 216 M\_MAA\_A3  
A1 72 M\_MAA\_A2  
A0 79 M\_MAA\_A0

SCL 141 SMB\_CLK\_DIMM  
SDA 285 SMB\_DATA\_DIMM

SA-2 238  
SA-1 140  
SA-0 139

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

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DIMM1 (CHANNEL-A)  
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DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

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M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

M\_DATA\_A[63:0] 3

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

VCC\_DDR

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VCC\_DDR

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VCC\_DDR

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DQ-63 280 M\_DATA\_A57  
DQ-62 136 M\_DATA\_A59  
DQ-61 273 M\_DATA\_A61  
DQ-60 128 M\_DATA\_A56  
DQ-59 282 M\_DATA\_A60  
DQ-58 137 M\_DATA\_A62  
DQ-57 275 M\_DATA\_A58  
DQ-56 130 M\_DATA\_A63  
DQ-55 269 M\_DATA\_A55  
DQ-54 124 M\_DATA\_A53  
DQ-53 262 M\_DATA\_A48  
DQ-52 117 M\_DATA\_A50  
DQ-51 271 M\_DATA\_A49  
DQ-50 126 M\_DATA\_A51  
DQ-49 264 M\_DATA\_A52  
DQ-48 119 M\_DATA\_A54  
DQ-47 258 M\_DATA\_A42  
DQ-46 113 M\_DATA\_A46  
DQ-45 261 M\_DATA\_A40  
DQ-44 108 M\_DATA\_A41  
DQ-43 260 M\_DATA\_A43  
DQ-42 115 M\_DATA\_A47  
DQ-41 253 M\_DATA\_A44  
DQ-40 108 M\_DATA\_A45  
DQ-39 247 M\_DATA\_A39  
DQ-38 102 M\_DATA\_A38  
DQ-37 240 M\_DATA\_A37  
DQ-36 96 M\_DATA\_A36  
DQ-35 249 M\_DATA\_A35  
DQ-34 104 M\_DATA\_A34  
DQ-33 242 M\_DATA\_A33  
DQ-32 97 M\_DATA\_A32  
DQ-31 188 M\_DATA\_A27  
DQ-30 43 M\_DATA\_A30  
DQ-29 181 M\_DATA\_A25  
DQ-28 36 M\_DATA\_A28  
DQ-27 190 M\_DATA\_A31  
DQ-26 45 M\_DATA\_A26  
DQ-25 183 M\_DATA\_A24  
DQ-24 38 M\_DATA\_A29  
DQ-23 177 M\_DATA\_A23  
DQ-22 32 M\_DATA\_A19  
DQ-21 170 M\_DATA\_A20  
DQ-20 25 M\_DATA\_A21  
DQ-19 179 M\_DATA\_A18  
DQ-18 34 M\_DATA\_A22  
DQ-17 172 M\_DATA\_A16  
DQ-16 27 M\_DATA\_A17  
DQ-15 166 M\_DATA\_A15  
DQ-14 21 M\_DATA\_A11  
DQ-13 159 M\_DATA\_A8  
DQ-12 14 M\_DATA\_A9  
DQ-11 168 M\_DATA\_A14  
DQ-10 23 M\_DATA\_A10  
DQ-9 161 M\_DATA\_A13  
DQ-8 16 M\_DATA\_A12  
DQ-7 155 M\_DATA\_A7  
DQ-6 10 M\_DATA\_A3  
DQ-5 148 M\_DATA\_A4  
DQ-4 3 M\_DATA\_A1  
DQ-3 157 M\_DATA\_A2  
DQ-2 12 M\_DATA\_A6  
DQ-1 150 M\_DATA\_A0  
DQ-0 5 M\_DATA\_A5

BG-1 207 M\_BG\_A\_1  
BG-0 63 M\_BG\_A\_0

BA-1 224 M\_BA\_A\_1  
BA-0 81 M\_BA\_A\_0

A16\_RAS\_N  
A15\_CAS\_N  
A14\_WE\_N

A17 234 M\_MAA\_A16  
A12 86 M\_MAA\_A15  
A11 228 M\_MAA\_A14  
A10 232 M\_MAA\_A13  
A9 65 M\_MAA\_A12  
A8 210 M\_MAA\_A11  
A7 225 M\_MAA\_A10  
A6 68 M\_MAA\_A9  
A5 68 M\_MAA\_A8  
A4 211 M\_MAA\_A7  
A3 69 M\_MAA\_A6  
A2 213 M\_MAA\_A5  
A1 71 M\_MAA\_A4  
A0 216 M\_MAA\_A3  
A1 72 M\_MAA\_A2  
A0 79 M\_MAA\_A0

SCL 141 SMB\_CLK\_DIMM  
SDA 285 SMB\_DATA\_DIMM

SA-2 238  
SA-1 140  
SA-0 139

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

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DIMM1 (CHANNEL-A)  
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DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

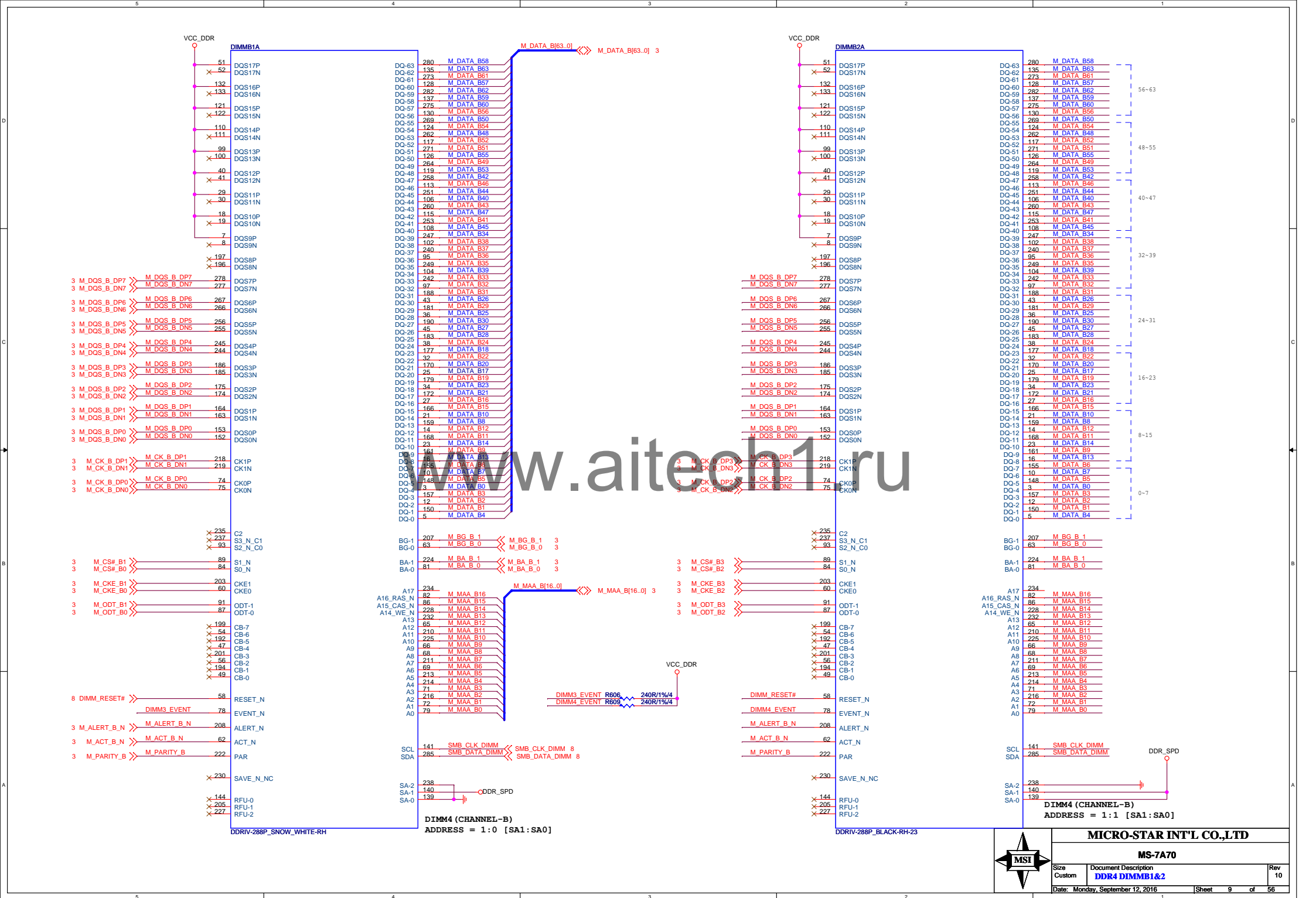
DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

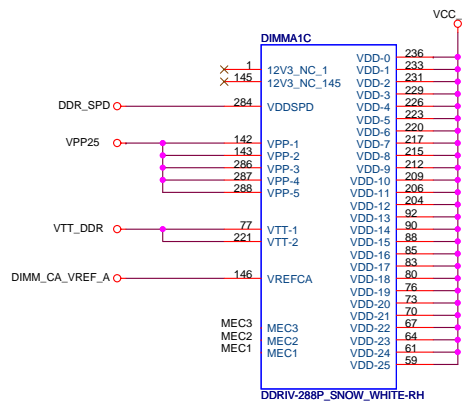
DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

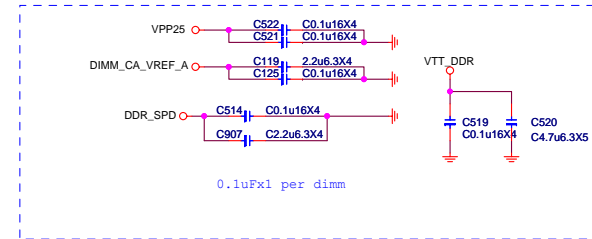
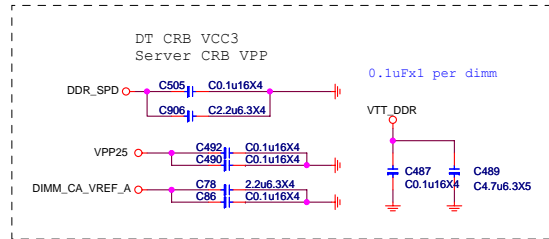
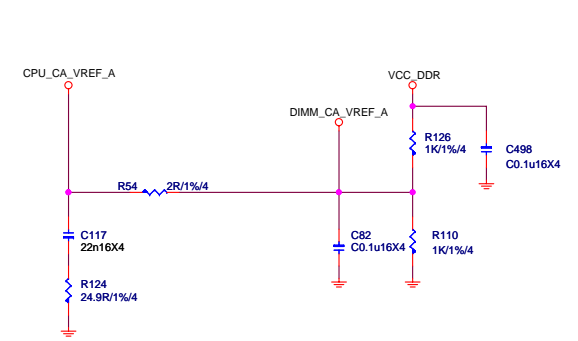
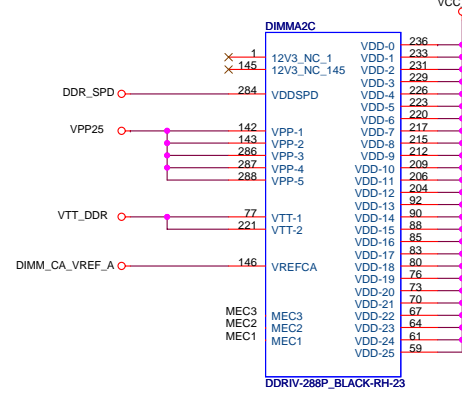
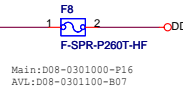
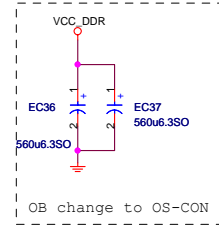
DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

DIMM1 (CHANNEL-A)  
ADDRESS = 0:0 [SA1:SA0]

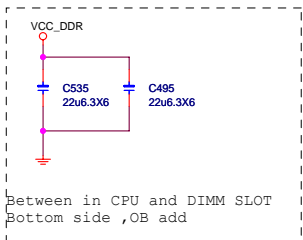
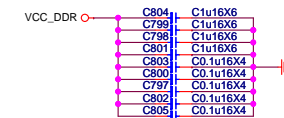
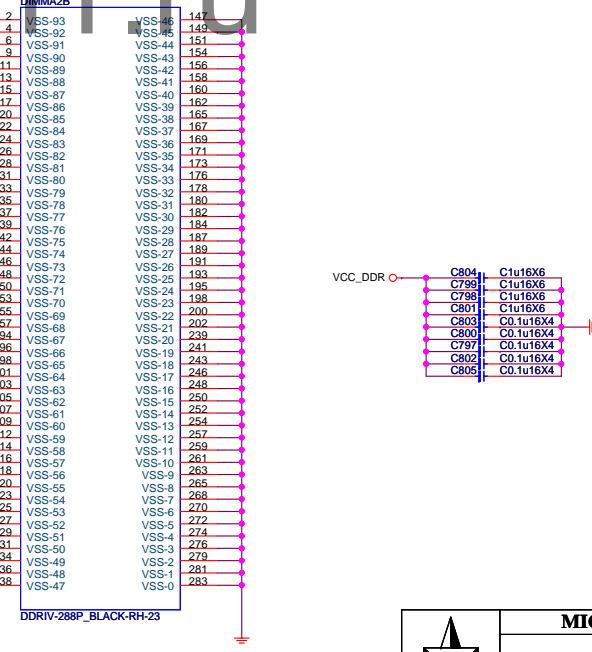
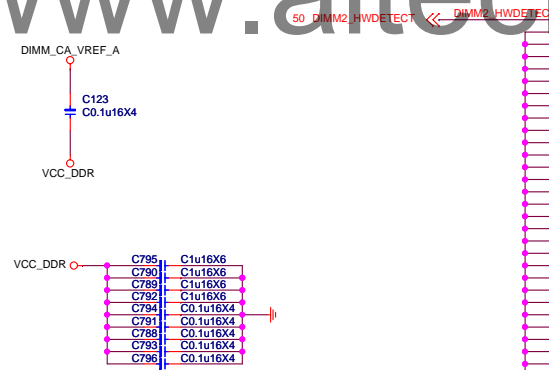
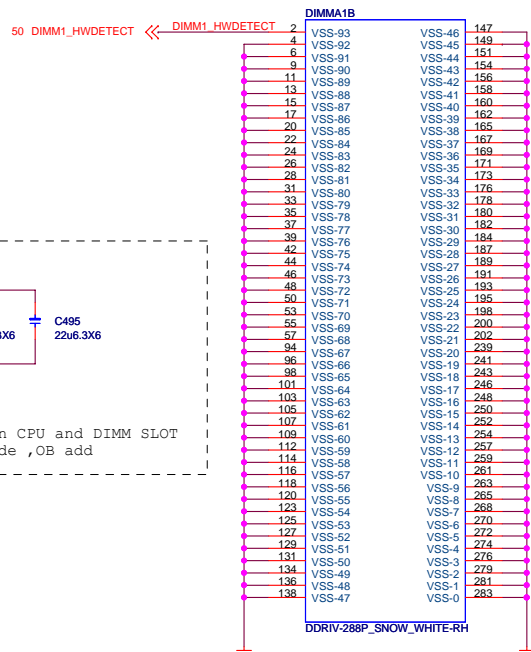




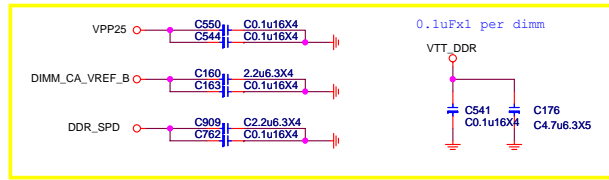
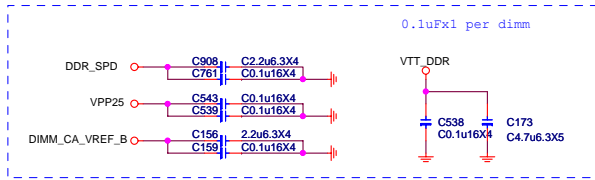
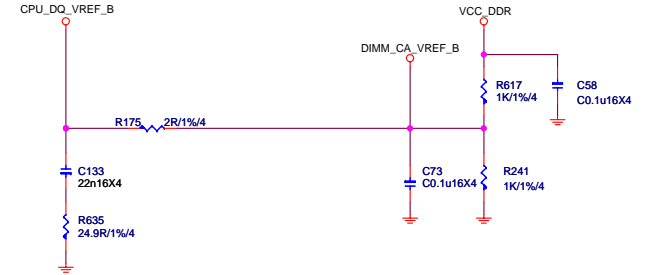
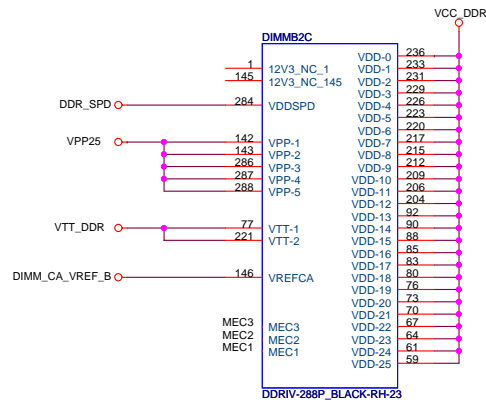
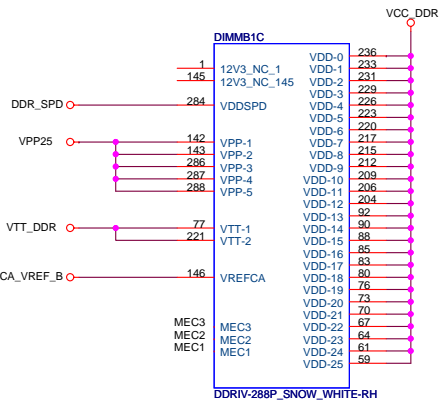
### DIMM SLOT PN BY SPEC



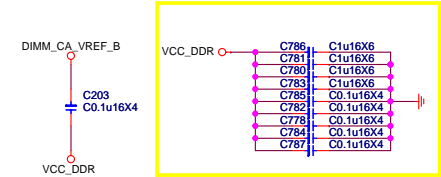
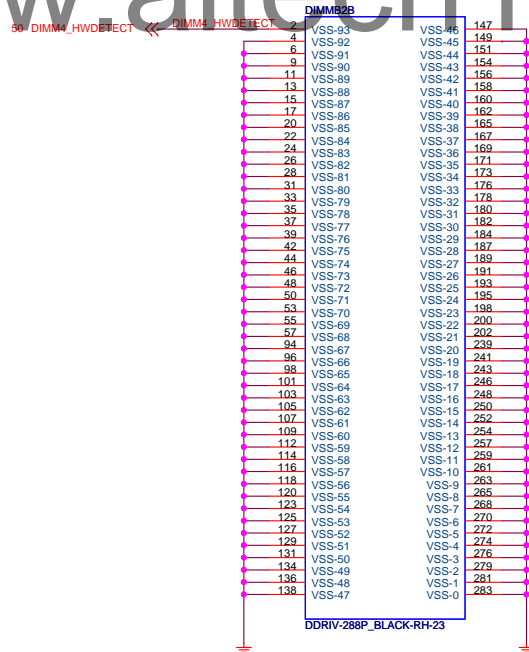
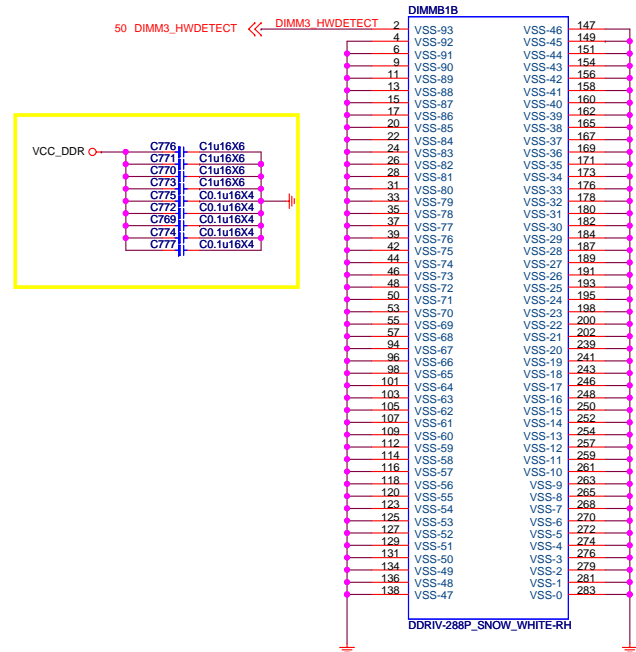
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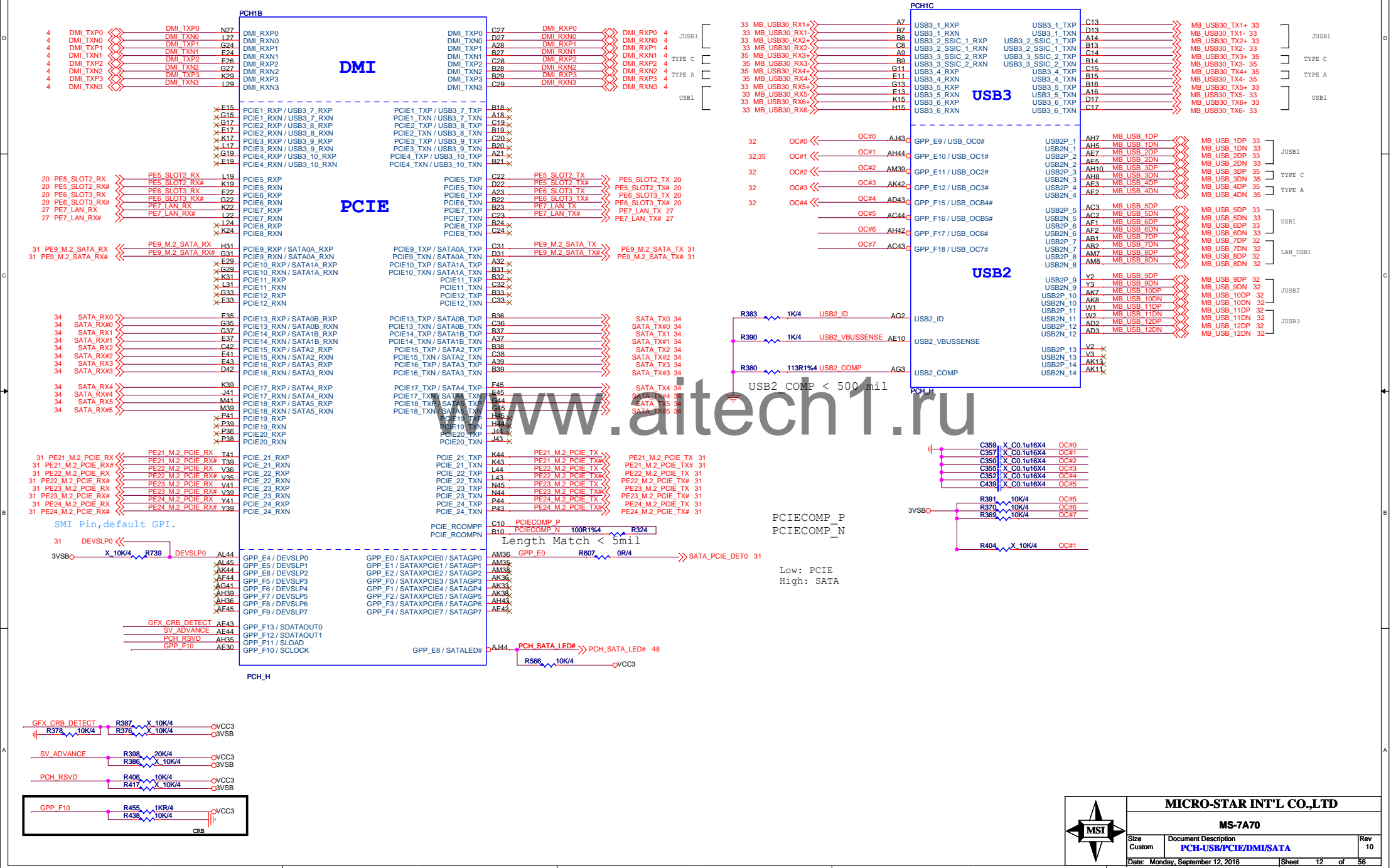


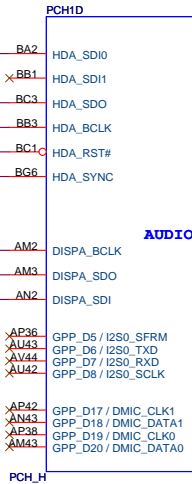
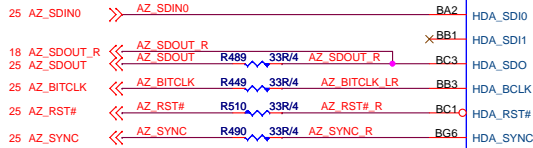
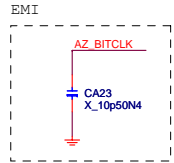


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GPP\_I[3:0] with SMI/NMI

PORT B

GPP\_I5 / DDPB\_CTRLCLK

GPP\_I6 / DDPB\_CTRLDATA



PORT C

GPP\_I7 / DDPC\_CTRLCLK

GPP\_I8 / DDPC\_CTRLDATA



PORT D

GPP\_I9 / DDPD\_CTRLCLK

GPP\_I10 / DDPD\_CTRLDATA



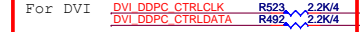
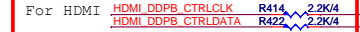
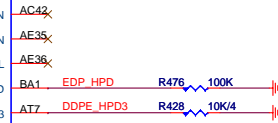
eDP

GPP\_F19 / eDP\_VDDEN

GPP\_F20 / eDP\_BKLTEN

GPP\_F21 / eDP\_BKLTCTL

GPP\_I3 / DDPE\_HP03



DDI interface Disable  
no connect

Port B HDMI

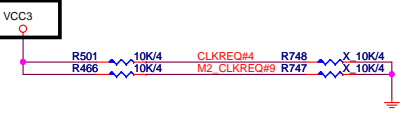
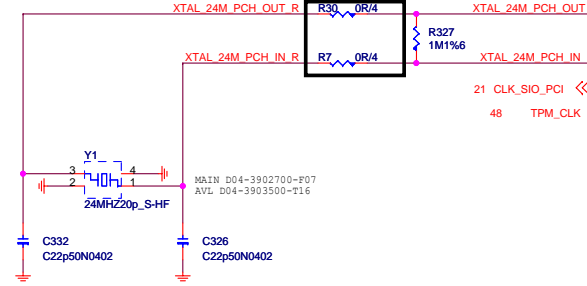
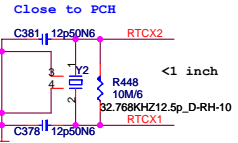
Port C DVI, HDMI2.0 OR Others

Port D DisplayPort

MAIN D04-0305901-F07

AVL D04-0306001-C11

AVL D04-0306101-T02



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PCH1E

GPP\_A9 / CLKOUT\_LPC0 / ESPL\_CLK

GPP\_A10 / CLKOUT\_LPC1

GPP\_A16 / CLKOUT\_48

LPC

RTC

24MHZ

CLK\_REQ

LAN

CLKREQ#4

M2\_CLKREQ#9

CLKREQ#4

M2\_CLKREQ#9

CLKREQ#4

M2\_CLKREQ#9

CLKREQ#4

M2\_CLKREQ#9

CLKREQ#4

M2\_CLKREQ#9

CLKREQ#4

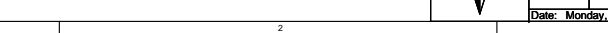
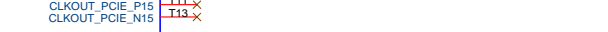
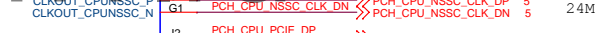
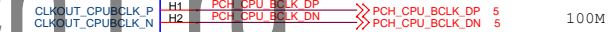
M2\_CLKREQ#9

CLKREQ#4

M2\_CLKREQ#9

CLKREQ#4

M2\_CLKREQ#9



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Date:	Monday, September 12, 2016	Sheet 13 of 56









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**MS-7A70**

Size	Custom
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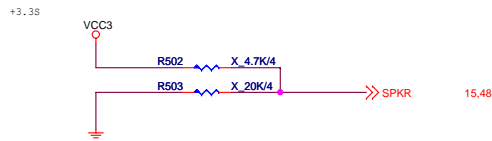
Document Description  
**PCH-GND**

Rev  
10

Date: Monday, September 12, 2016

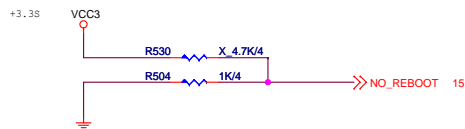
Sheet 17 of 56

# TOP Swap



Internal pull-down 20K is disabled after PLTRST#

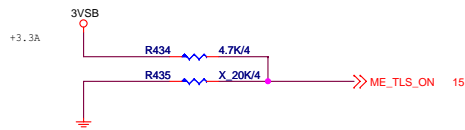
# No Reboot



0 : DISABLE (Default)  
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

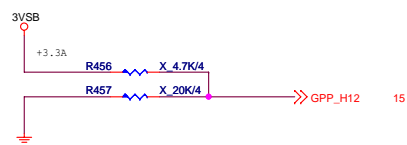
# AMT and SBA with confidentiality



0 : DISABLE  
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

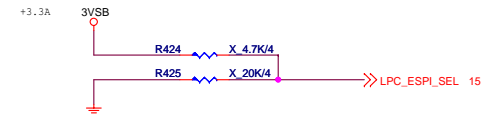
# ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING  
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

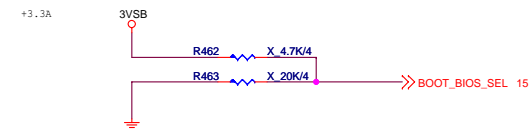
# LPC eSPI Mode



0 : LPC  
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

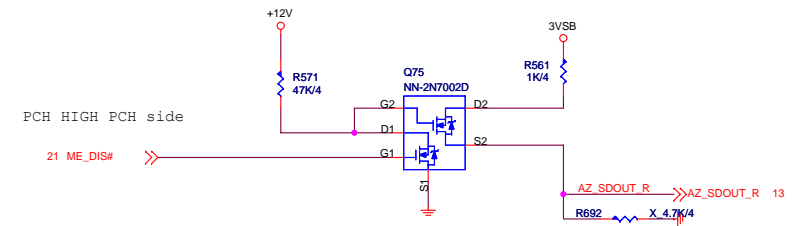
# Boot BIOS



0 : SPI  
1 : LPC

Internal pull-down 20K is disabled after PLTRST

# HDA\_SDO



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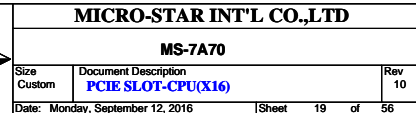
MS-7A70

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**LED**  
: DOC-040P100-H91  
**AVL**: DOC-040S500-E07

LED  
 7 : DOC-040T200-H91  
 AVL: DOC-040S200-E07  
 PCIE SLOT LED



2015.6.8 change net\_name to SMBCLK\_VSB and SMBDATA\_VSB

15,19 SMBCLK\_VSB\_R  
15,19 SMBDATA\_VSB\_R

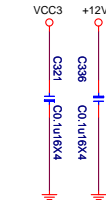
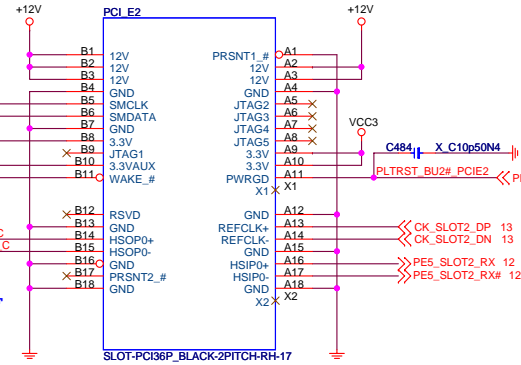
2014.12.29

12 PE5\_SLOT2\_TX  
12 PE5\_SLOT2\_TX#

C329 0.22u6.3X4  
C330 0.22u6.3X4

PE5\_SLOT2\_TX\_C  
PE5\_SLOT2\_TX#\_C

H110 only GEN2 stuff 0.1uF  
B150 Support GEN3 stuff 0.22uF



2016.1.12 add C321 C336

2015.6.8 change net\_name to SMBCLK\_VSB and SMBDATA\_VSB

15,19 SMBCLK\_VSB\_R  
15,19 SMBDATA\_VSB\_R

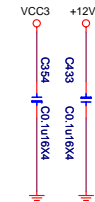
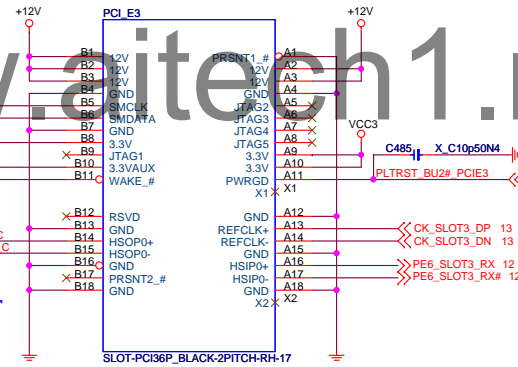
2014.12.29

12 PE6\_SLOT3\_TX  
12 PE6\_SLOT3\_TX#

C374 0.22u6.3X4  
C375 0.22u6.3X4

PE6\_SLOT3\_TX\_C  
PE6\_SLOT3\_TX#\_C

H110 only GEN2 stuff 0.1uF  
B150 Support GEN3 stuff 0.22uF



2015.6.16 add C65

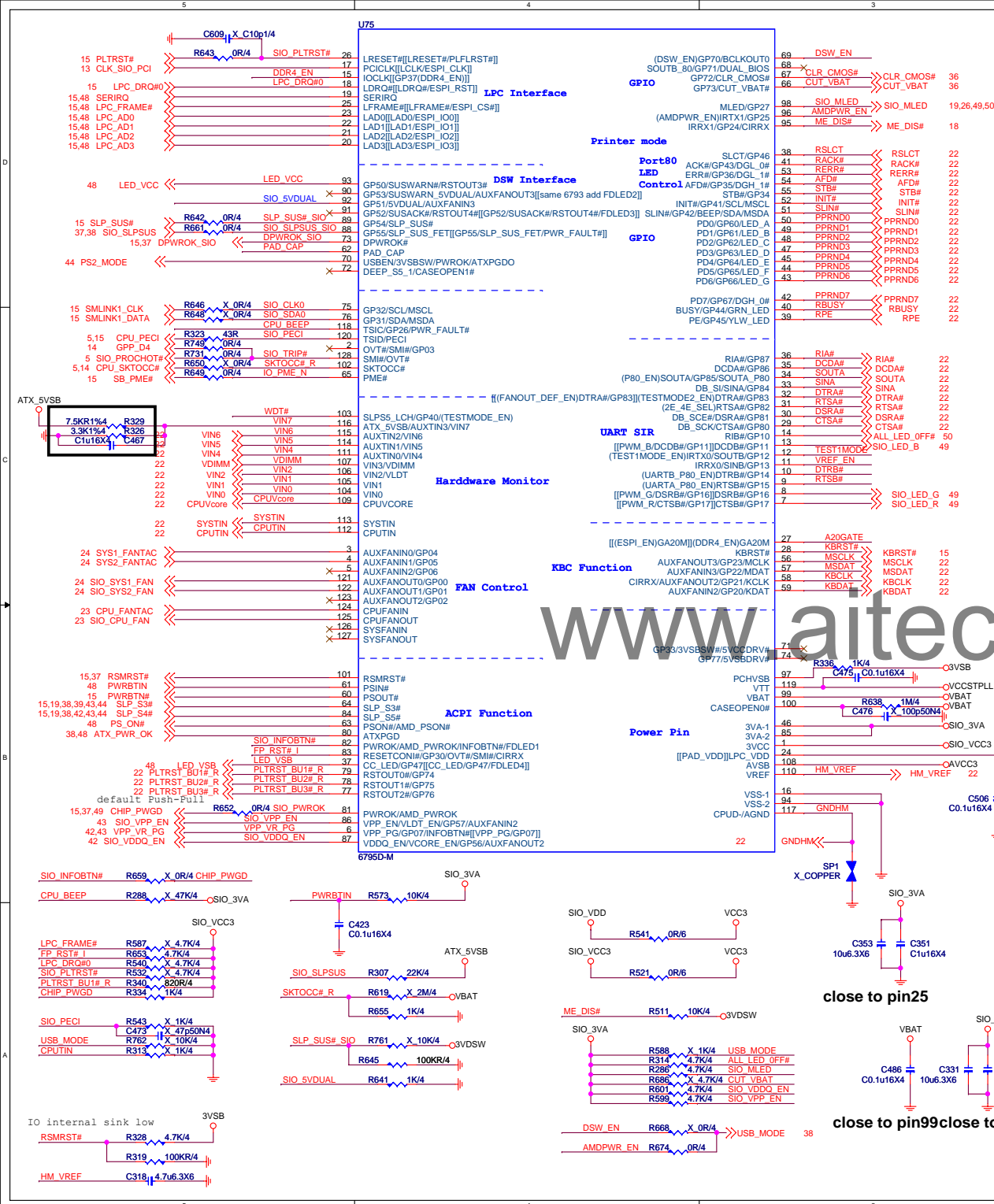
2016.1.12 add C354 C433



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## POWER ON STRAPPING PIN FOR NCT6793/6795

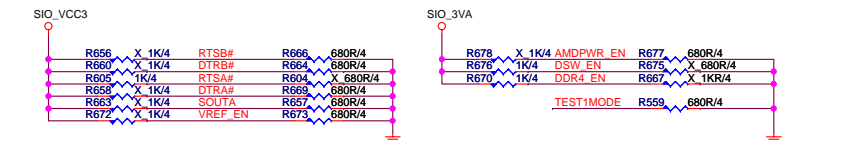
PIN 6793/6795 NAME		Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:

If PIN34 strapping low, BIOS must programming LPT or GPIO

### SIO Pin Strap

(PIN31)RTSA#	0=2E	1=4E
(PIN32)DTRA#	0=24MHz	1=48MHz
(PIN34)SOUTA	0=Port80 Enable	1=PRT Enable
(PIN69)DSW_EN	0=Disable	1=Enable
(PIN9) (RTSB#)ORT80_EN	0=Disable	1=Enable
(PIN96)AMDPWR_EN	0=Disable	1=Enable
(PIN62) (SLP_S5_LCH#)TEST_MODE_EN	0=Disable	1=Enable



Pin diagram for the HZT1326M\_BLACK-RH package. The package is shown with pins 1 through 25 on the left and pins 2 through 24 on the right. Pin 1 is RSTB#, pin 2 is RAFD#, pin 3 is PRND0, pin 4 is RERR#, pin 5 is PRND1, pin 6 is RINIT#, pin 7 is PRND2, pin 8 is RSLIN#, pin 9 is PRND3, pin 10 is an unlabeled pin, pin 11 is PRND4, pin 12 is an unlabeled pin, pin 13 is PRND5, pin 14 is an unlabeled pin, pin 15 is PRND6, pin 16 is an unlabeled pin, pin 17 is PRND7, pin 18 is an unlabeled pin, pin 19 is RACK#, pin 20 is an unlabeled pin, pin 21 is RBUSY, pin 22 is an unlabeled pin, pin 23 is RPE, pin 24 is an unlabeled pin, and pin 25 is RSLCT. The package is labeled HZT1326M\_BLACK-RH.

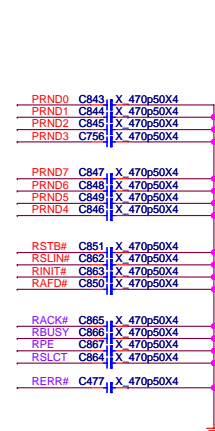
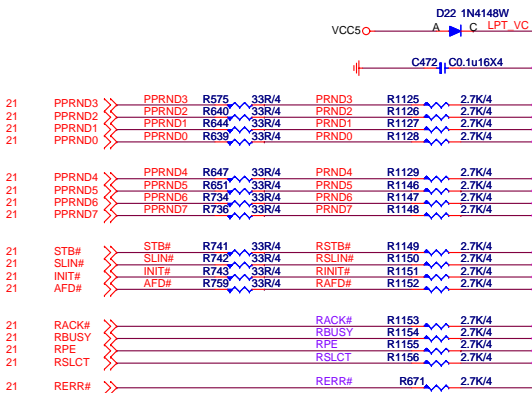
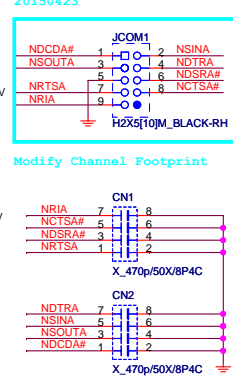
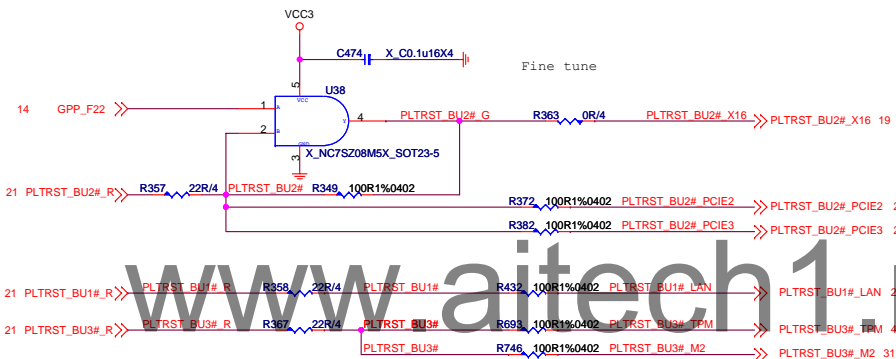
[illegible][illegible]

Figure 10 illustrates the typical power supply circuit diagram, showing connections for various power rails and their associated components:

- VCORE:** Connected to R303 (10K1%4) and CPUVcore. A parallel combination of R364 (X\_10K1%4) and C319 (10u6.3X6) is connected to ground.
- +12V:** Connected to R315 (220K1%4) and VIN0. A parallel combination of R321 (20K1%4) and C325 (C0.1u16X4) is connected to ground.
- VDD\_DDR:** Connected to R680 (10KR1%4) and VDIMM. A parallel combination of R682 (10K1%4) and C479 (10u6.3X6) is connected to ground.
- VCCIO:** Connected to R683 (10K1%4) and VIN4. A parallel combination of R683 and C480 (10u6.3X6) is connected to ground.
- VCC5:** Connected to R306 (12K1%4) and VIN1. A parallel combination of R316 (3K1%4) and C324 (C0.1u16X4) is connected to ground.
- PCH\_1VSB:** Connected to R305 (10KR1%4) and VIN2. A parallel combination of R305 and C507 (10u6.3X6) is connected to ground.
- VCCSA:** Connected to R684 (10KR1%4) and VINS. A parallel combination of R684 and C481 (10u6.3X6) is connected to ground.
- VGT:** Connected to R685 (10K1%4) and VIN6. A parallel combination of R685 and C482 (10u6.3X6) is connected to ground.

[illegible]

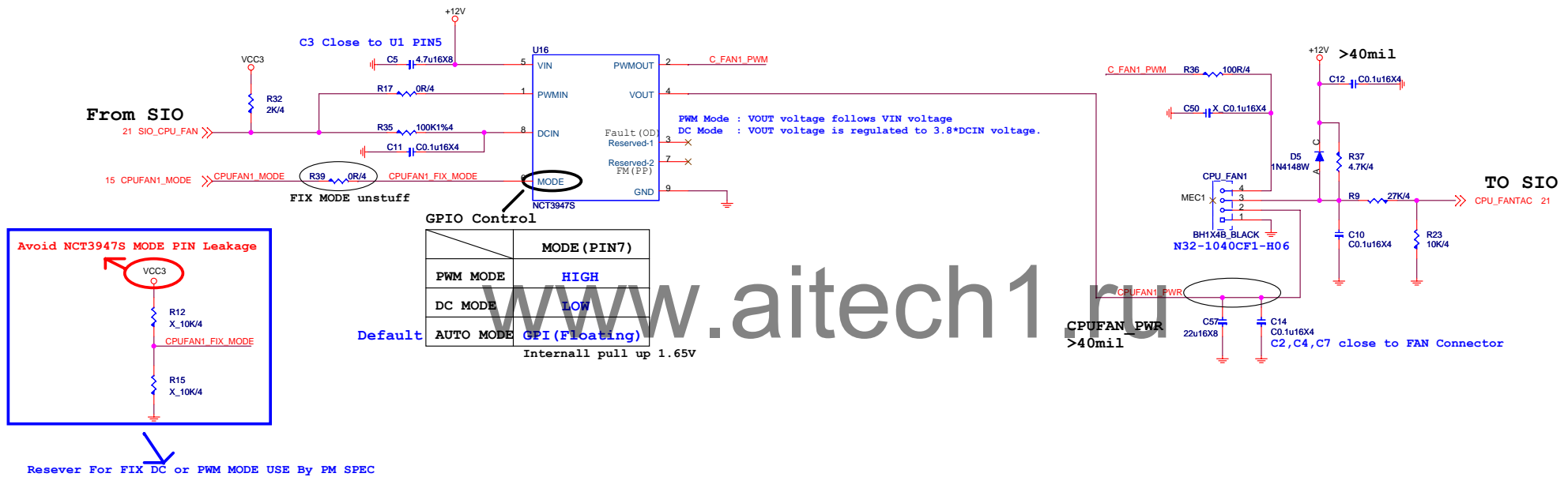
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# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

## 2.GPIO パBIOSち伝 PWM/DC MODE

TYPE K



TYPE K

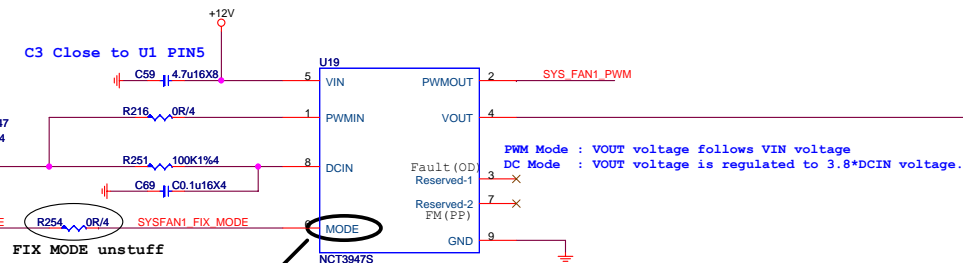
From SIO

21 SIO\_SYS1\_FAN

15 SYSFAN1\_MODE

Avoid NCT3947S MODE PIN Leakage

Resever For FIX DC or PWM MODE USE By PM SPEC

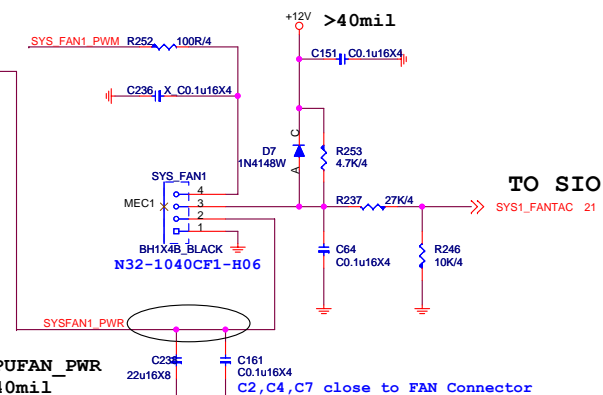


Default

Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO バイオスち伝 PWM/DC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO バイオスち伝 PWM/DC MODE

TYPE K

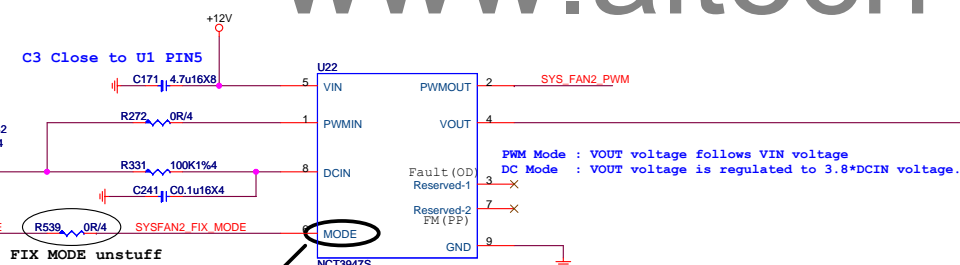
From SIO

21 SIO\_SYS2\_FAN

15 SYSFAN2\_MODE

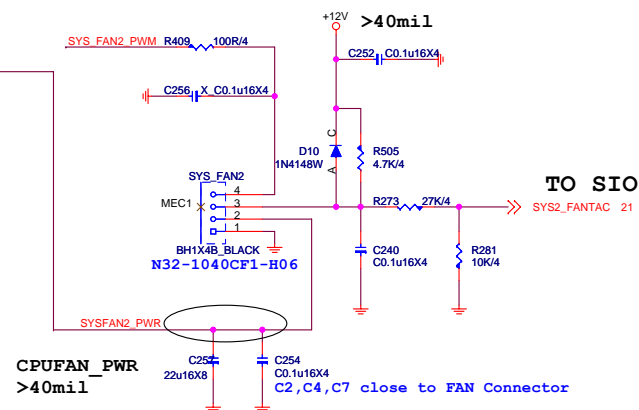
Avoid NCT3947S MODE PIN Leakage

Resever For FIX DC or PWM MODE USE By PM SPEC



Default

Internall pull up 1.65V

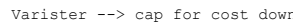
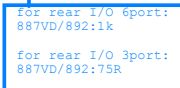
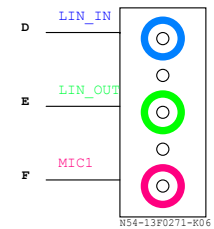
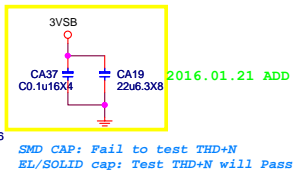


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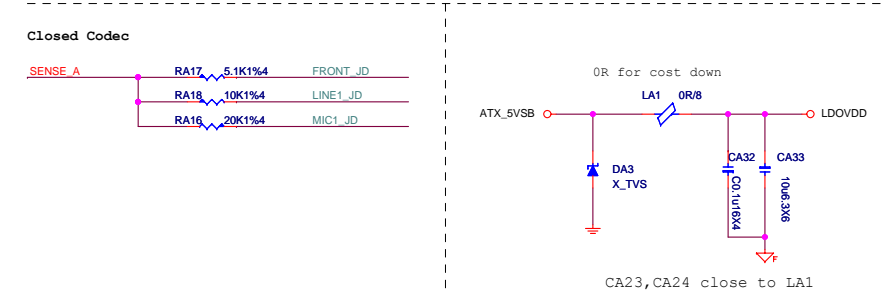
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Custom	FAN CONTROLLER	10
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## 2014.09.15



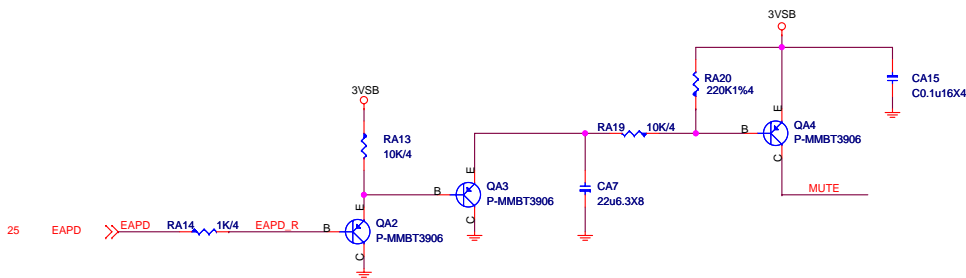
<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7A70</b>			
Size Custom	Document Description <b>AUDIO - ALC892/887</b>		Rev 10
Date: Monday, September 12, 2016		Sheet 25 of 56	





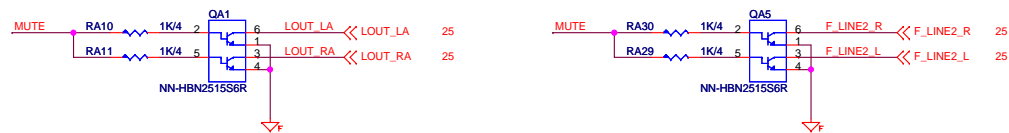
## Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

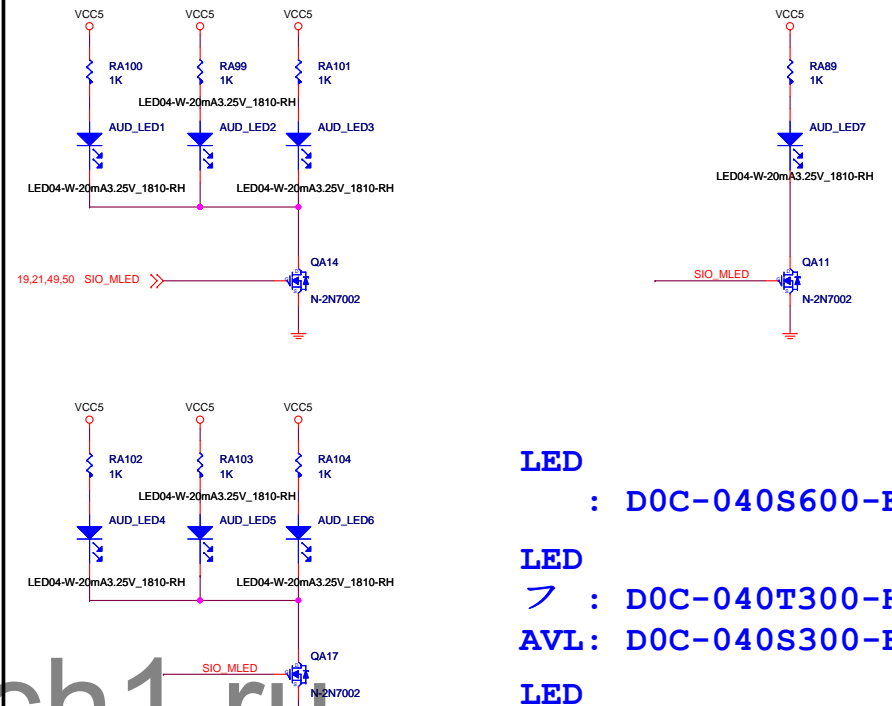


Digital

Analog



## AUDIO LED



LED : D0C-040S600-E07  
 LED : D0C-040T300-H91  
 AVL: D0C-040S300-E07  
 LED : D0C-040R700-H91

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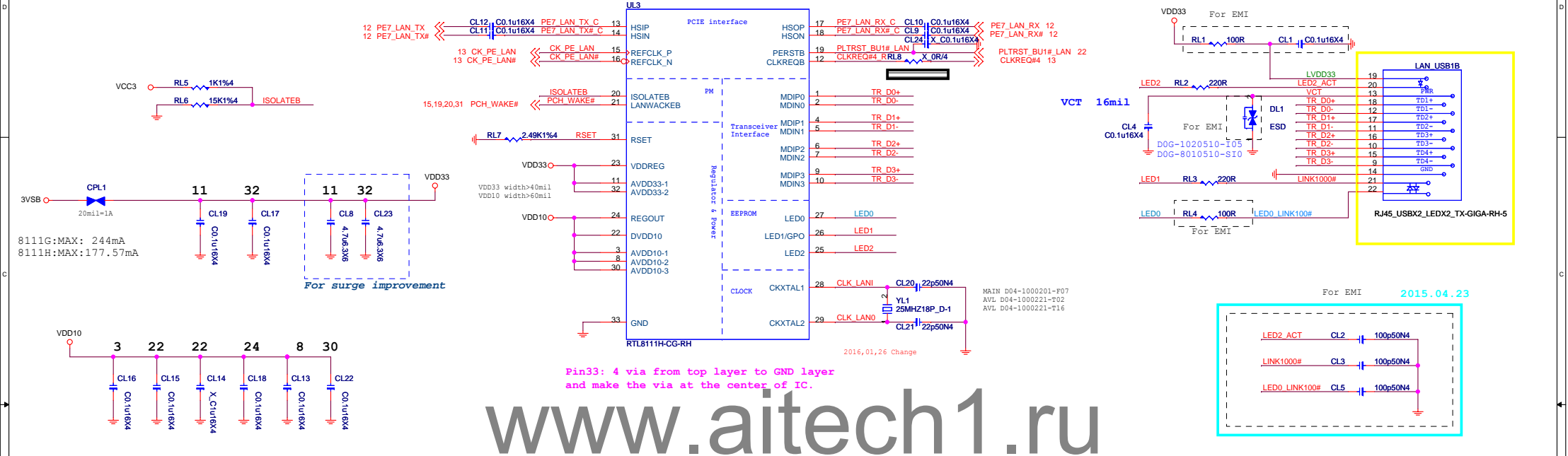
MS-7A70

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# RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09  
8111G:B06-081116C-R09

## LAN Connector



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8111G POWER Consumption

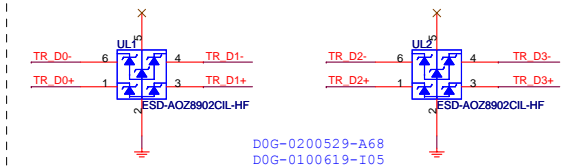
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

## ESD Protect

UL2&UL3 close to connector

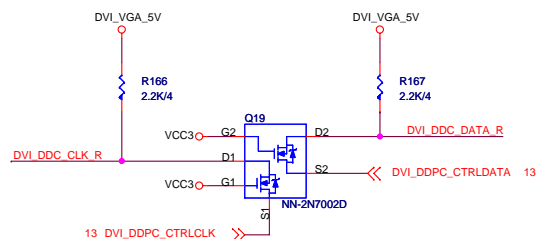


# DVI level shifter

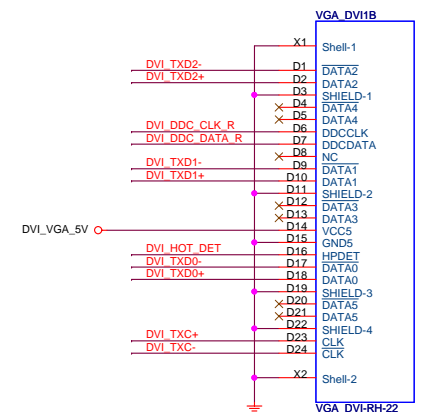
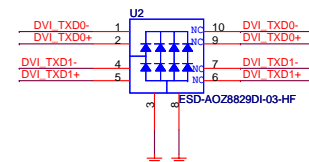
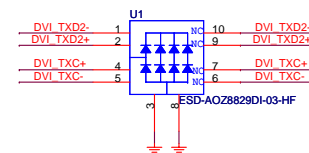
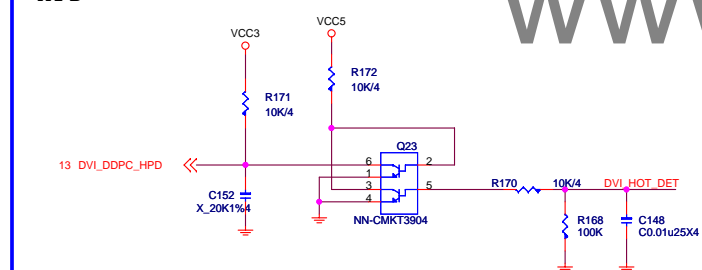
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



2015.01.11



HPD

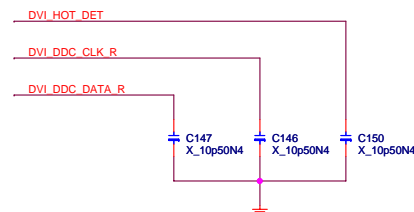
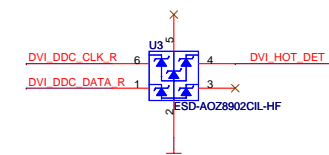
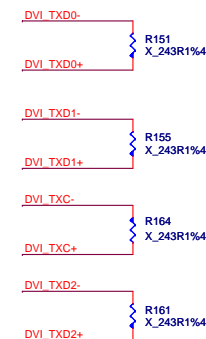


2015.10.19

N5B-24F0641-R06 -> N5B-24F0661-EB6

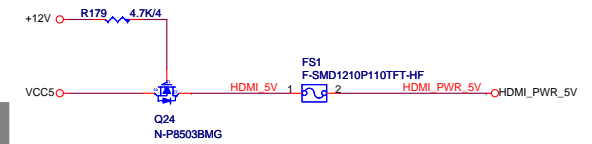
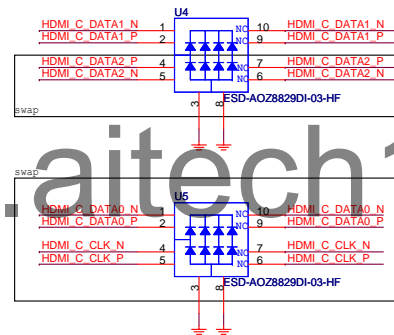
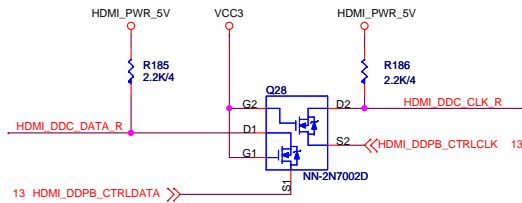
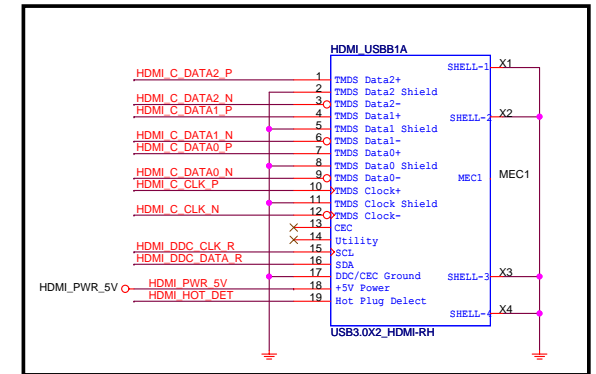
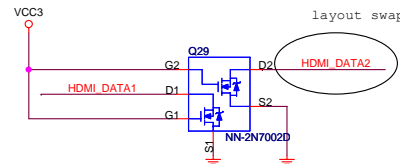
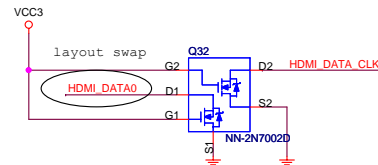
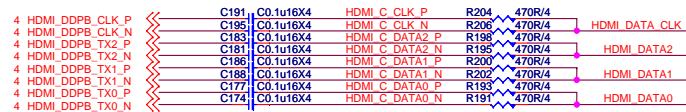


For EMI

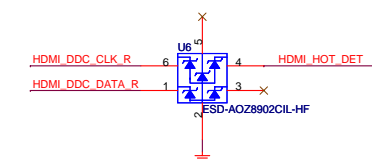
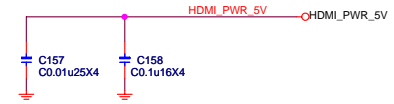
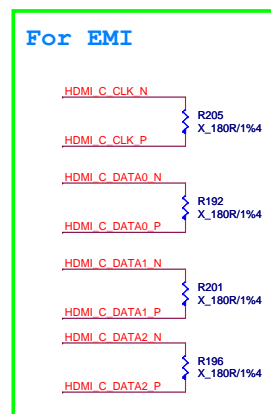
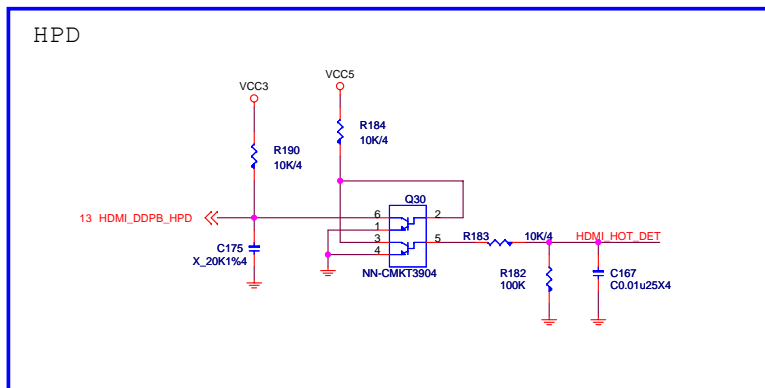


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HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

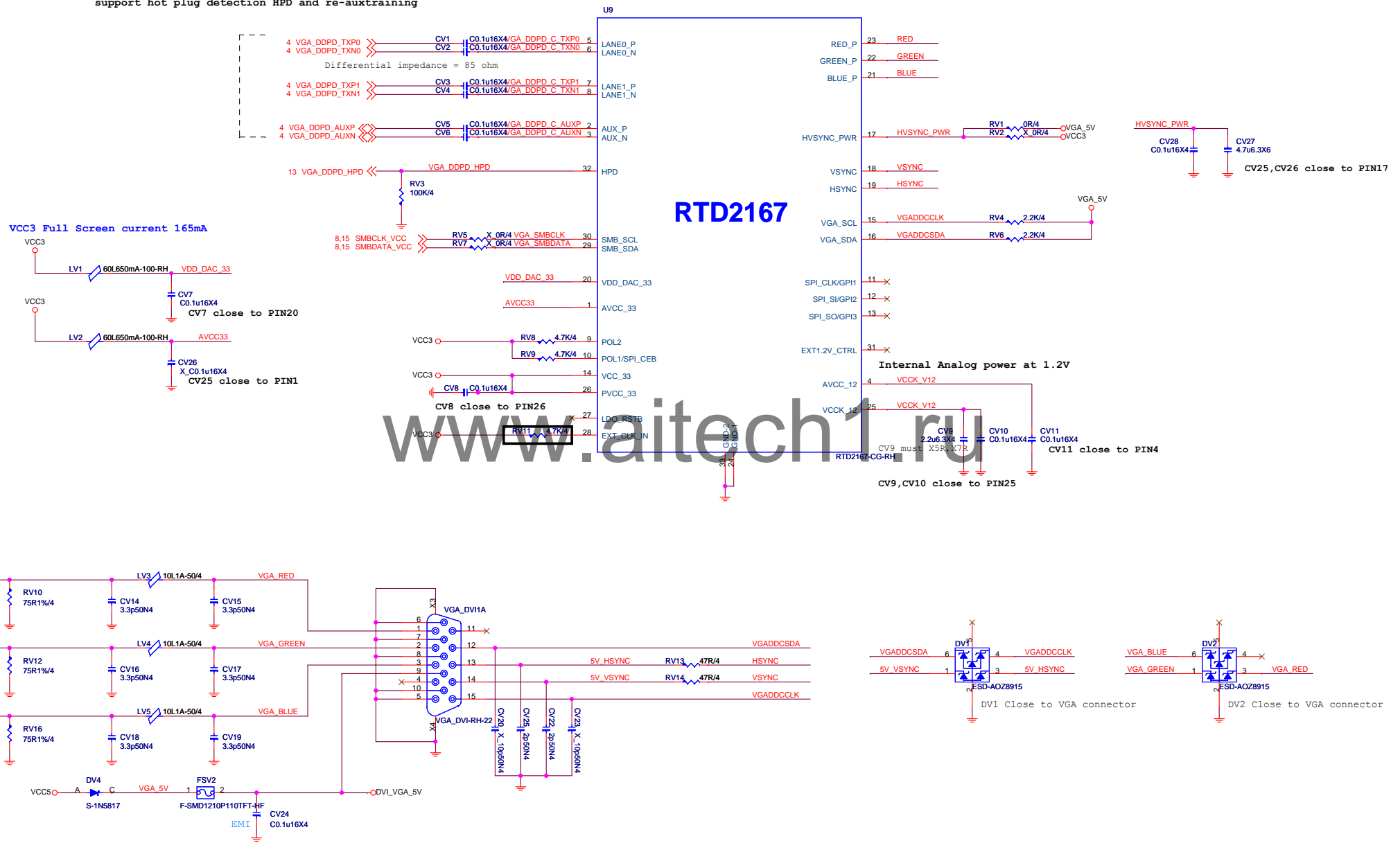


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**Note:**

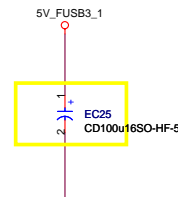
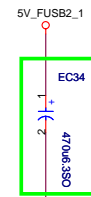
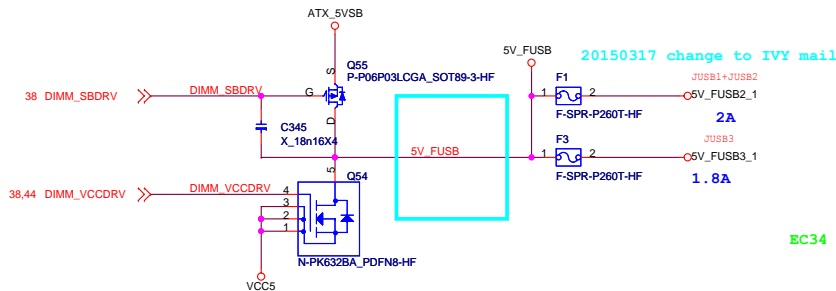
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



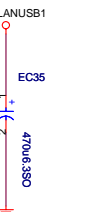
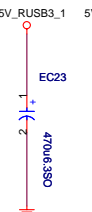
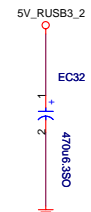
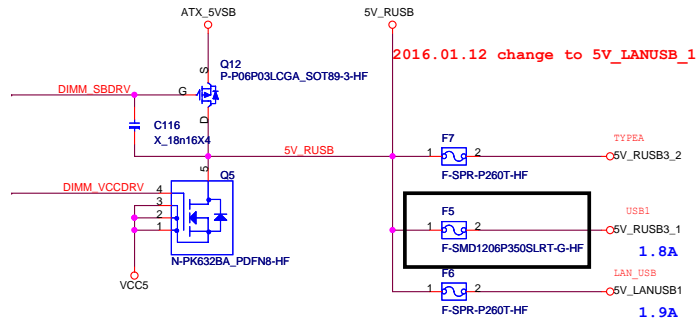
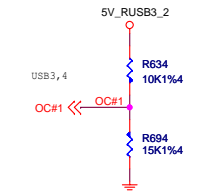
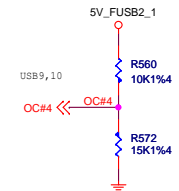
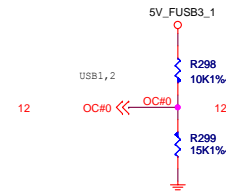
**MICRO-STAR INT'L CO.,LTD**

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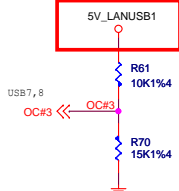
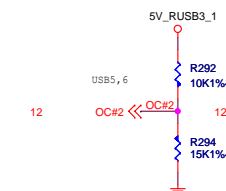




EC34 -> 560uF



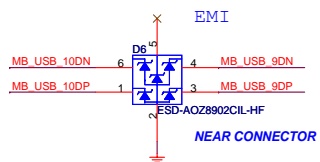
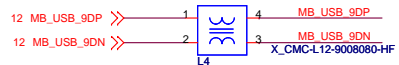
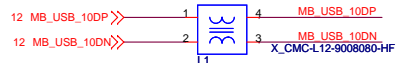
2015.05.28 Remove USB CAP EC3



2016.01.12 change to 5V\_LANUSB\_1&change to OC#3

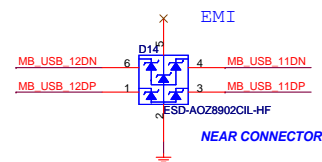
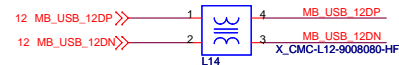
## FRONT USB PORT 9,10

2016.04.01



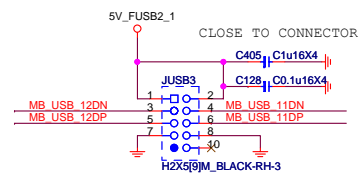
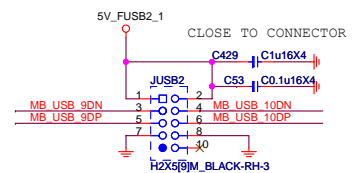
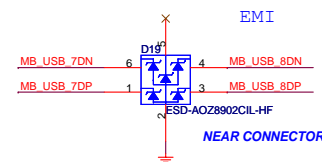
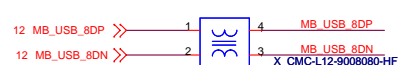
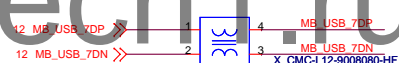
## FRONT USB PORT 11,12

2016.04.01

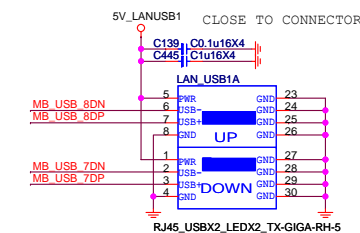


## REAR USB PORT 5,6

2016.04.01



2015.05.22 JUSB2 change to USB11,12  
PS2\_USB change to USB5,6

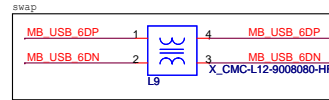
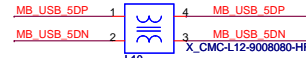
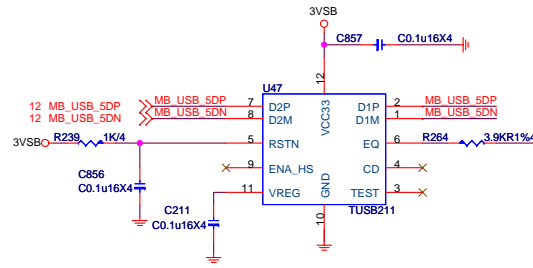


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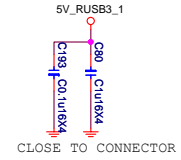
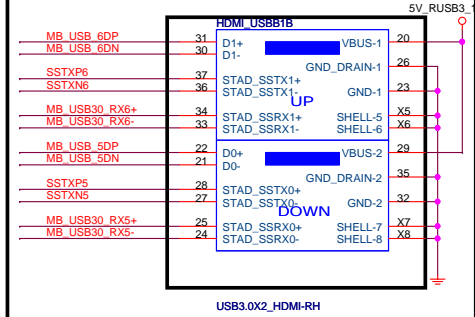
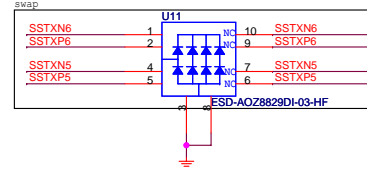
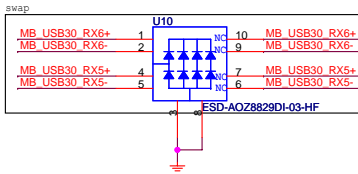
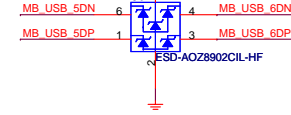
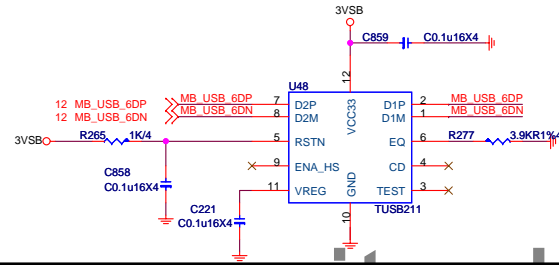
12 MB\_USB30\_TX5+ >>> C164 C0.1u16X4 SSTXP5  
12 MB\_USB30\_TX5- >>> C165 C0.1u16X4 SSTXN5

12 MB\_USB30\_RX5+ >>>  
12 MB\_USB30\_RX5- >>>



12 MB\_USB30\_TX6+ >>> C153 C0.1u16X4 SSTXP6  
12 MB\_USB30\_TX6- >>> C154 C0.1u16X4 SSTXN6

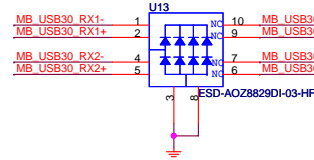
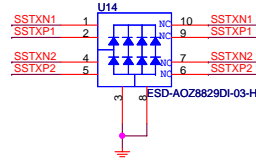
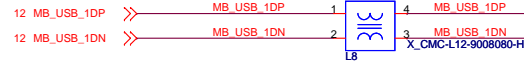
12 MB\_USB30\_RX6+ >>>  
12 MB\_USB30\_RX6- >>>



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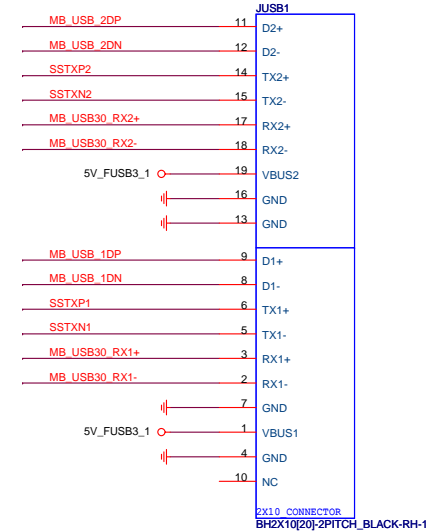
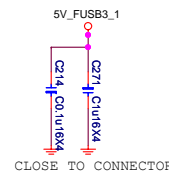
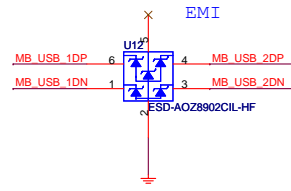
12 MB\_USB30\_TX1+ >>> C92 C0.1u16X4 SSTXP1  
12 MB\_USB30\_TX1- >>> C93 C0.1u16X4 SSTXN1

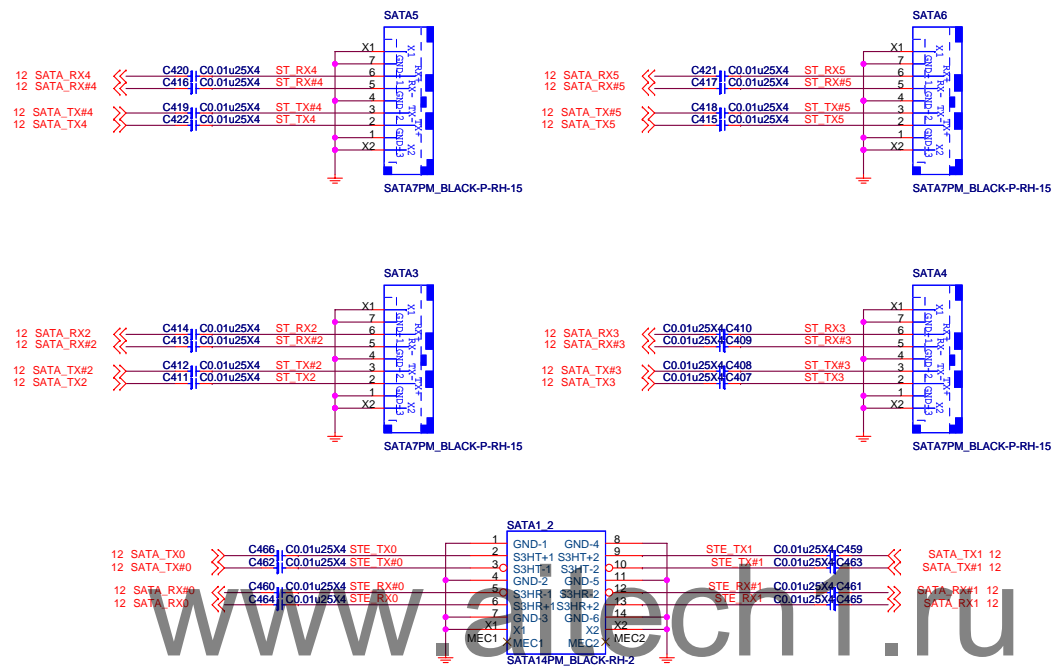
12 MB\_USB30\_RX1+ >>>  
12 MB\_USB30\_RX1- >>>



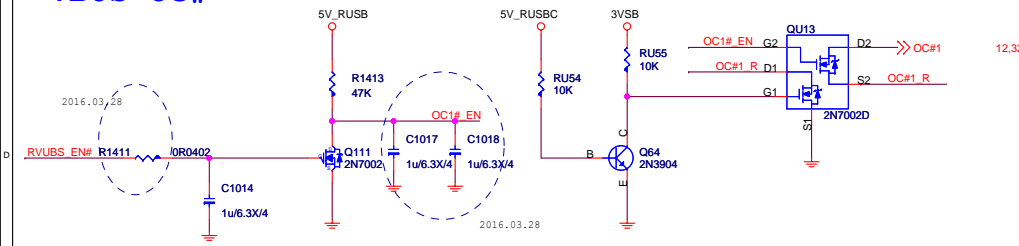
12 MB\_USB30\_TX2+ >>> C94 C0.1u16X4 SSTXP2  
12 MB\_USB30\_TX2- >>> C95 C0.1u16X4 SSTXN2

12 MB\_USB30\_RX2+ >>>  
12 MB\_USB30\_RX2- >>>

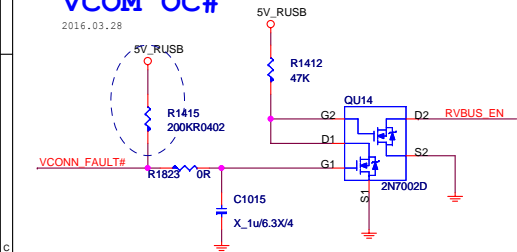




## VBUS OC#

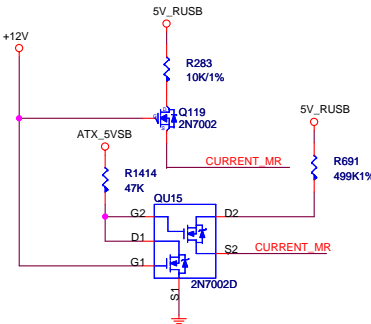


## VCOM OC#

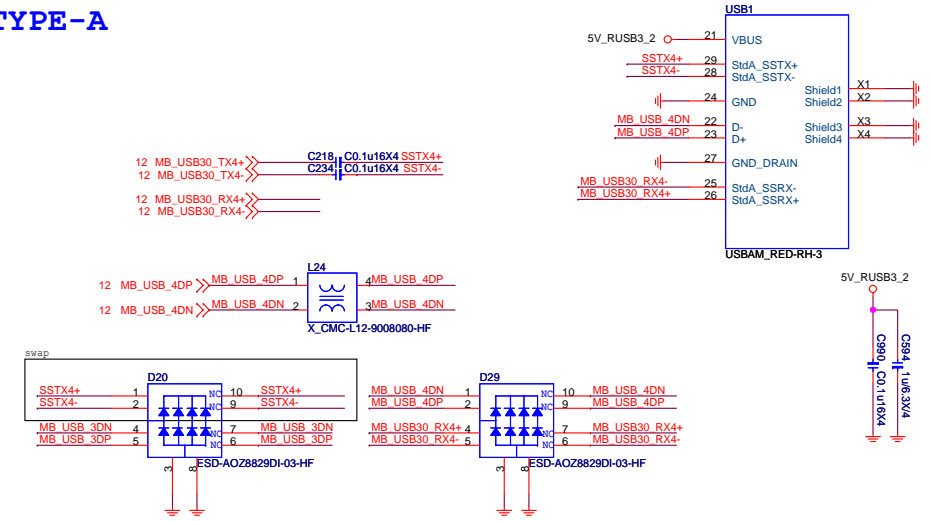


## Current Mode

L - Default for 900mA  
M - Mid (500K) for 1.5A  
H - High (10K) for 3A

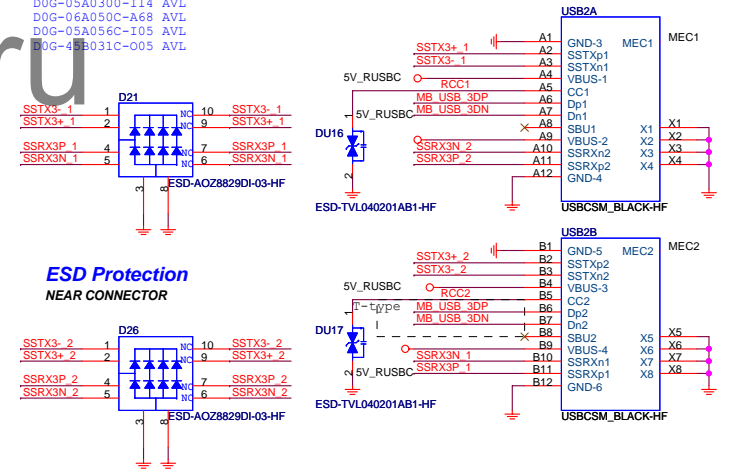


## TYPE-A

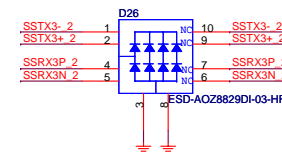


## TYPE-C

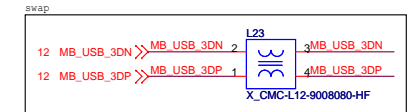
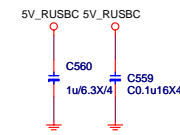
USB3.0  
D0G-06A030C-A68 Main  
D0G-05A0300-I14 AVL  
D0G-06A050C-A68 AVL  
D0G-05A056C-I05 AVL  
D0G-45B031C-005 AVL



## ESD Protection NEAR CONNECTOR

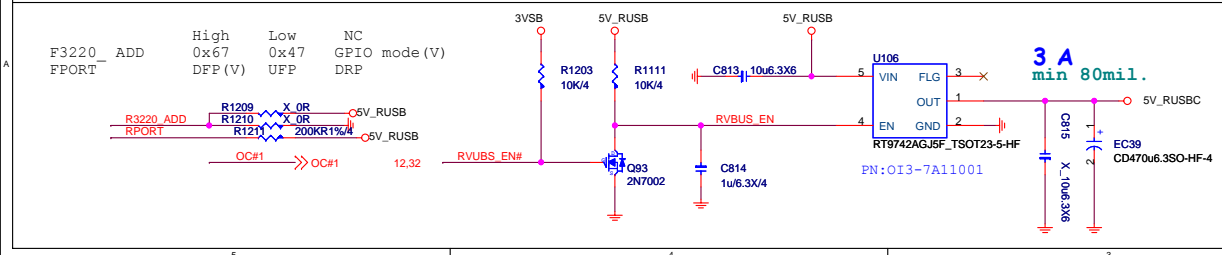
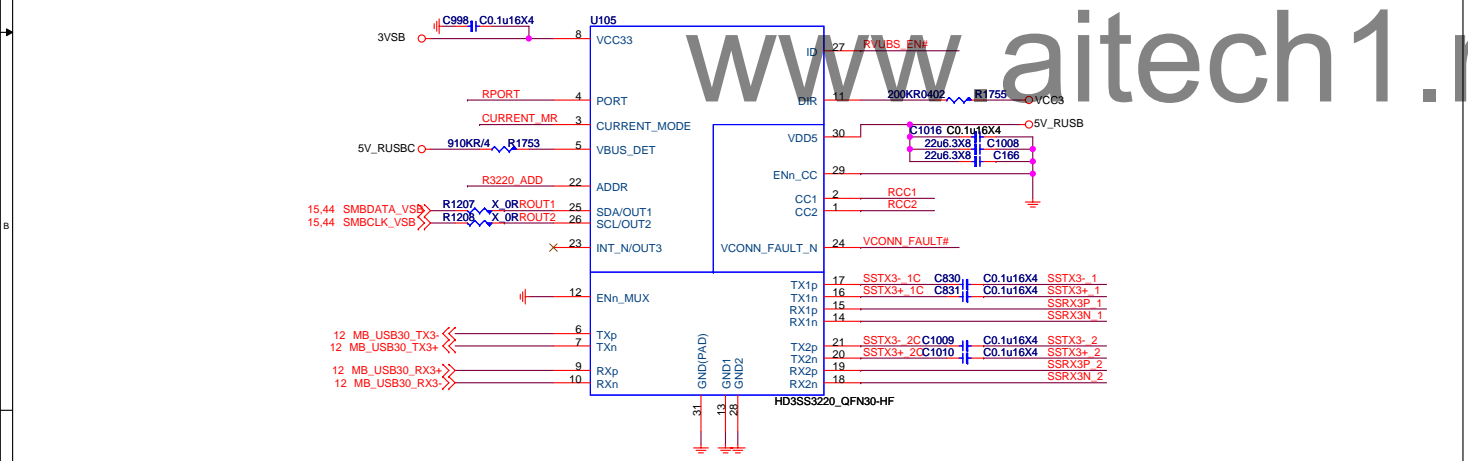


close to Type C Connector



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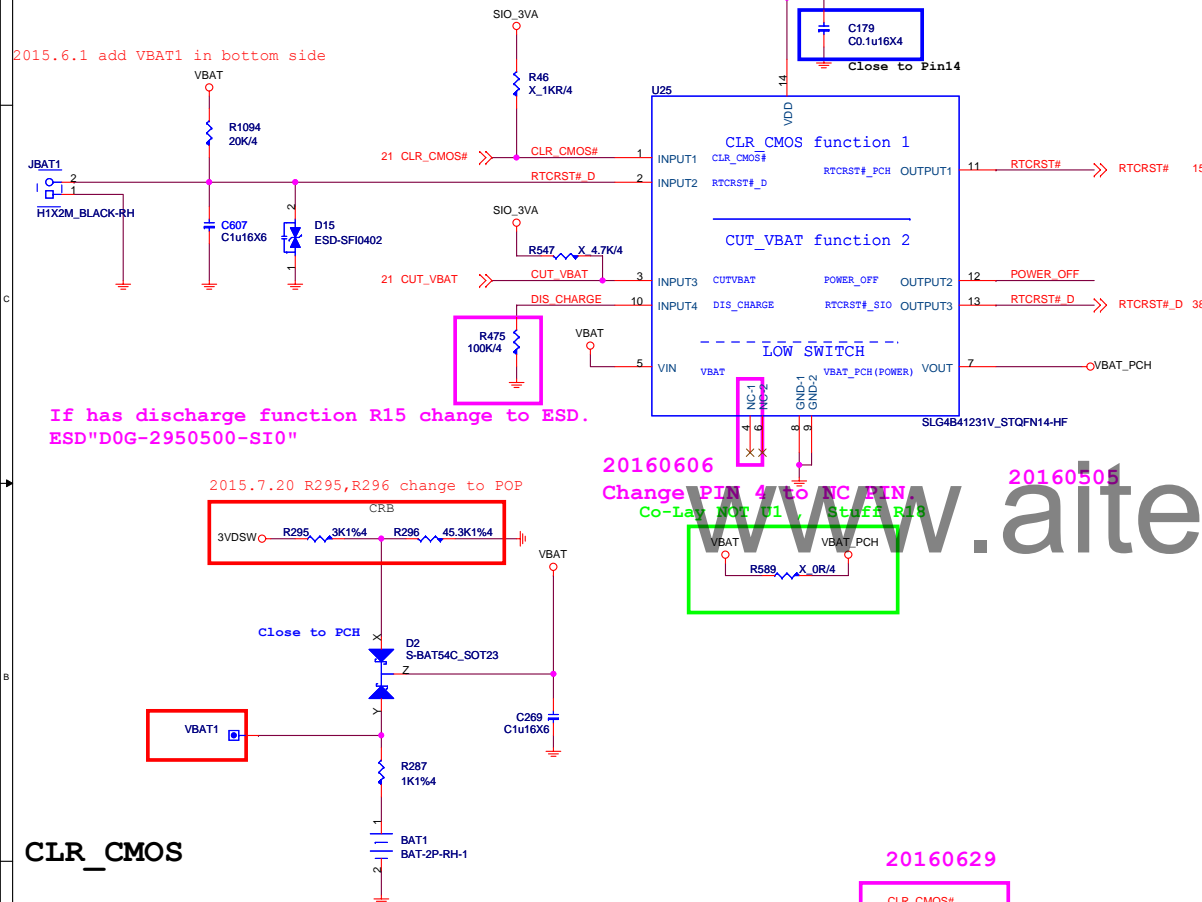


Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

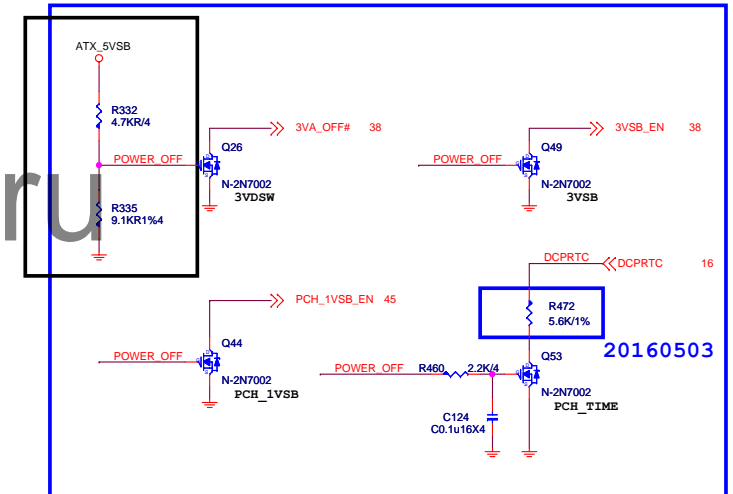
Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

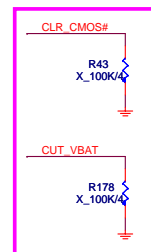
Default



Co-Lay NOT USE U1, ALL UNSTUFF



20160629



MICRO-STAR INT'L CO.,LTD

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15 PCH\_SPI0\_IO2 << PCH\_SPI0\_IO2  
15 PCH\_SPI0\_IO3 << PCH\_SPI0\_IO3

15 PCH\_SPI0\_CS0# << PCH\_SPI0\_CS0#  
15 PCH\_SPI0\_CLK << PCH\_SPI0\_CLK  
15 PCH\_SPI0\_MISO << PCH\_SPI0\_MISO  
15 PCH\_SPI0\_MOSI << PCH\_SPI0\_MOSI

SPI CS# < 25pF  
D0G-0402510-S10

2014.08.25

Close to JSP11

C399 C0.1u16X4

3VSB

3VSB

JSP11

PCH\_SPI0\_MISO

PCH\_SPI0\_CS0#

SPI\_SW\_SEL

PCH\_SPI0\_IO2

PCH\_SPI0\_MOSI

PCH\_SPI0\_CLK

PCH\_SPI0\_IO3

R2X8T0JM-2PITCH\_BLACK-RH-3

ATX\_5VSB

R548 10K/4

SPI\_SW\_SEL

Fine tune for SA reset

15,21 RSMRST#

R553 200R/4

RSMRST# R

S-RB751V-40\_SOD323-RH

D17

15,21,49 CHIP\_PWGD

S-RB751V-40\_SOD323-RH

D16

15,21 DPWROK\_SIO

X\_S-RB751V-40\_SOD323-RH

D25

21,38 SIO\_SLPSUS

S-RB751V-40\_SOD323-RH

For TL624-1.1 (SKYLAKE)  
In skylake, PCH core is powered by VSB which need sink RSMRST#  
to low by SPI\_SW\_SEL.

For TL624-1.1 : Stuff D4  
Old : Only RSVD (Because 12V level)

For TL624-1.1 : Stuff R493  
Old : Don't stuff R493

For TL624-1.1 : Stuff R494  
Old : Don't stuff R494

2014.12.15

3VSB

PCH\_SPI0\_MISO

R551 X 1K/4

PCH\_SPI0\_MOSI

R583 X 1K/4

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3VSB

R494 X 2.2K/4

3VSB

3VSB

C387 C0.1u16X4

C392 10u6.3X6

2015.01.15

2014.09.24 For intel MOW36 update

pull down resistor on SPI0\_IO3 is needed for SKL S/H  
platforms with pre-ES1/ES1 samples.

20150115

update this issue for PRE-ES2/ES2 refer mail 20150115  
From syng

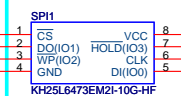
2015.05.27 SPI\_IO3 floating

\* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002

\* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset), component Q14.G Pull-high to ATX\_5VSB, Q14 must  
select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30

2015.04.23

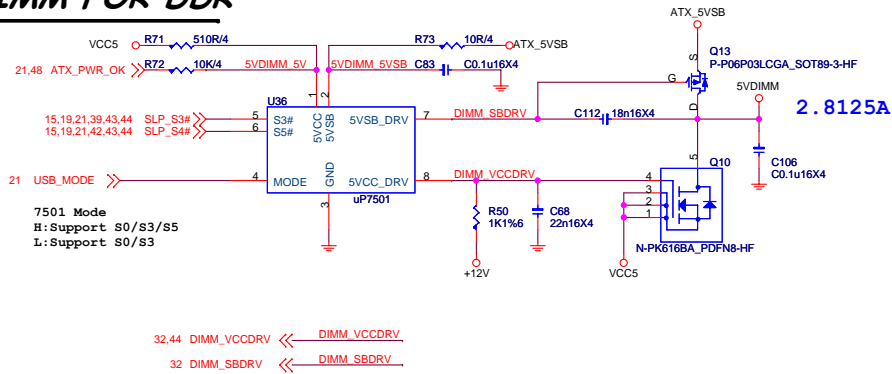


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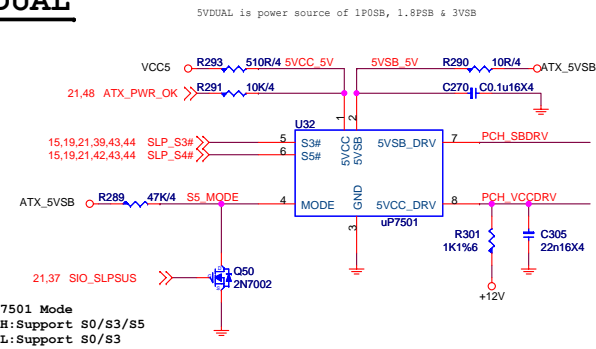
MS-7A70

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Custom	BIOS ROM	10
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## 5VDIMM FOR DDR

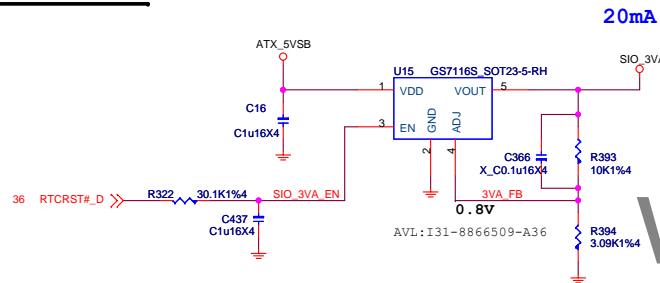


## 5VDUAL

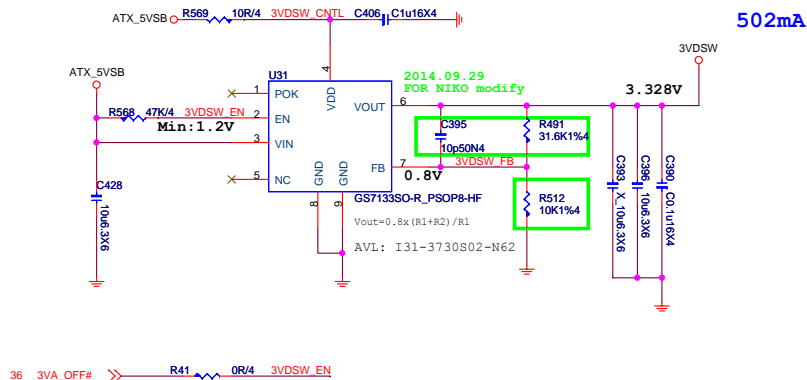


2015.09.15

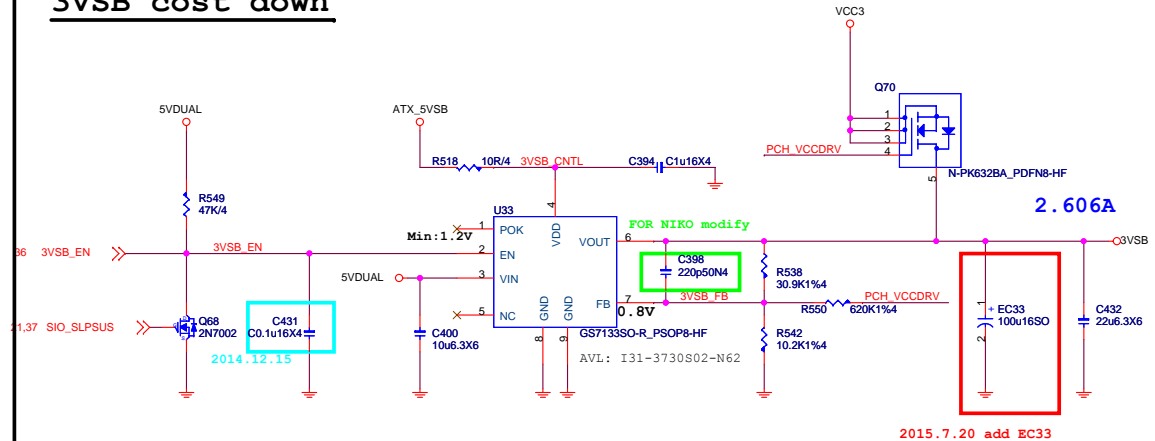
## SIO\_3VA



## 3VDSW



## 3VSB cost down



2015.7.20 add EC33



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Vcpu (SVID)=100A  
VGT (SVID)=48A

For driver Gate Mos Use

CRB 1.0 update  
RSVD R582  
2014.09.24

2015.7.20 R90 change to 36.5K

2015.08.04 change  
to C11-4757322-S02

2015.7.20  
R129 change to 150K  
R139 change to 15K

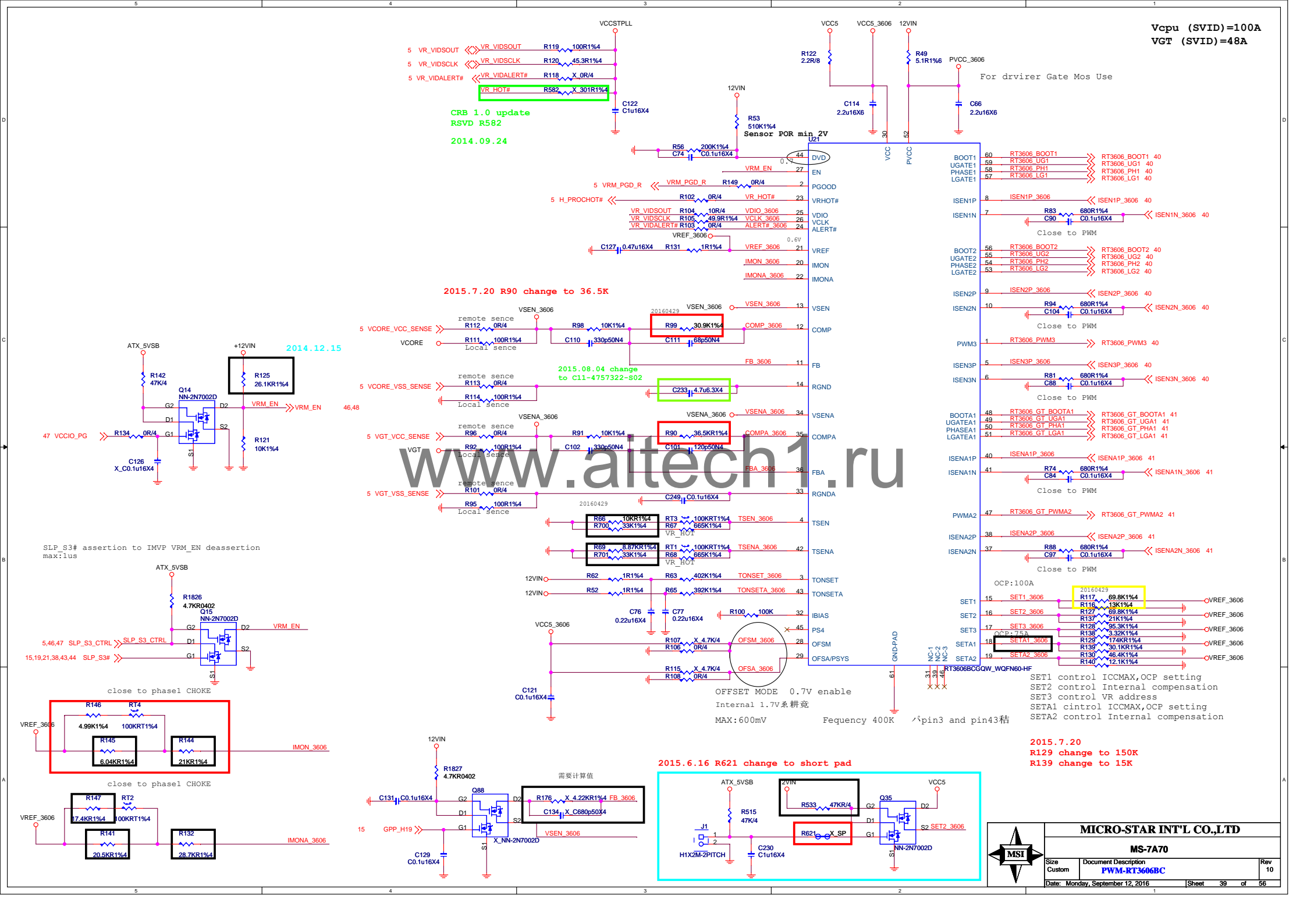
2015.6.16 R621 change to short pad

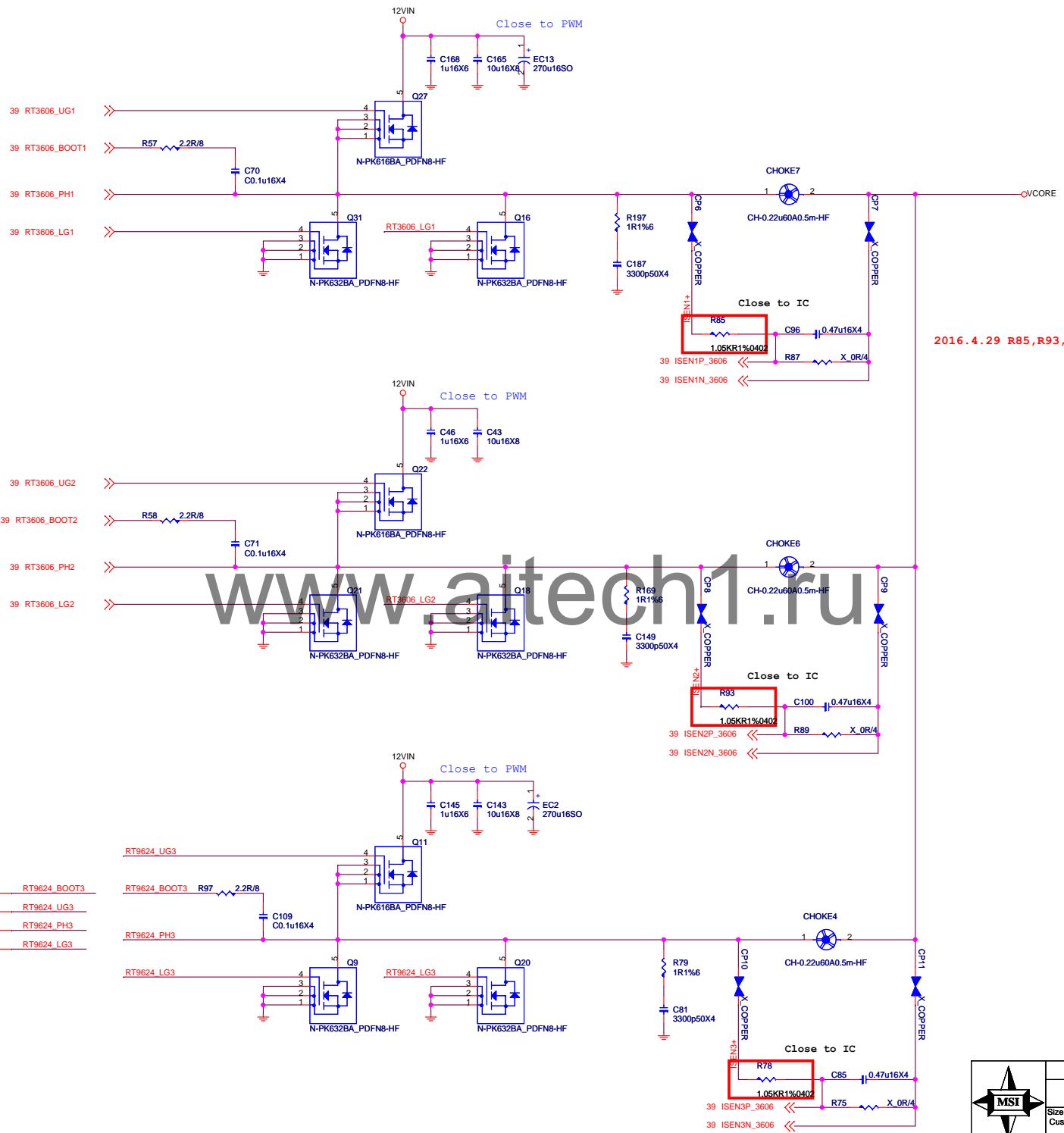


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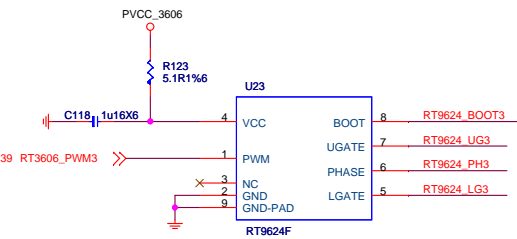
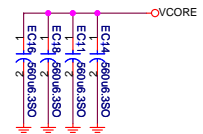
Size	Document Description	Rev
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ICCMAX: 79A  
LL: 2.1m ohm

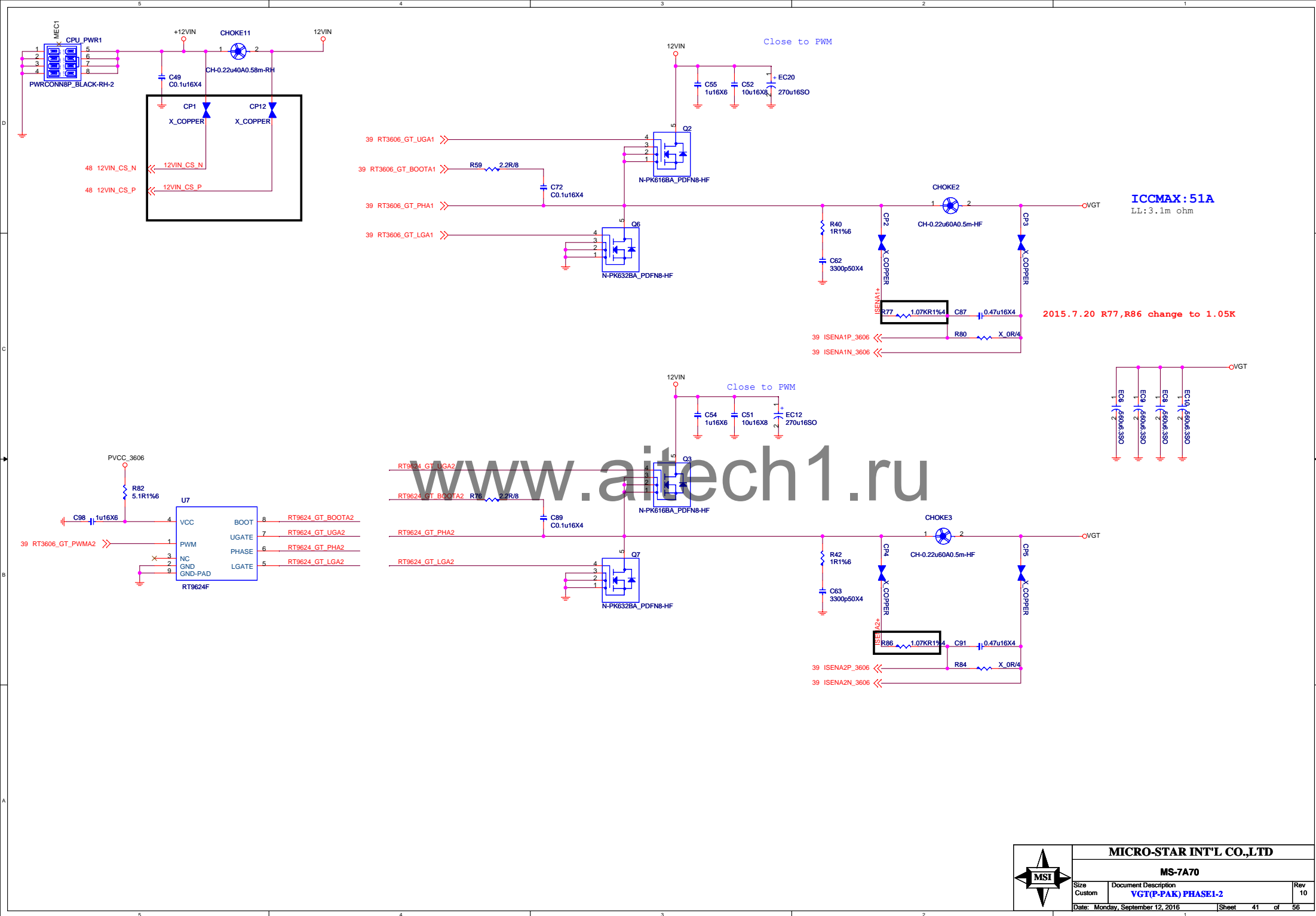
2016.4.29 R85,R93,R78 change to 1.05K

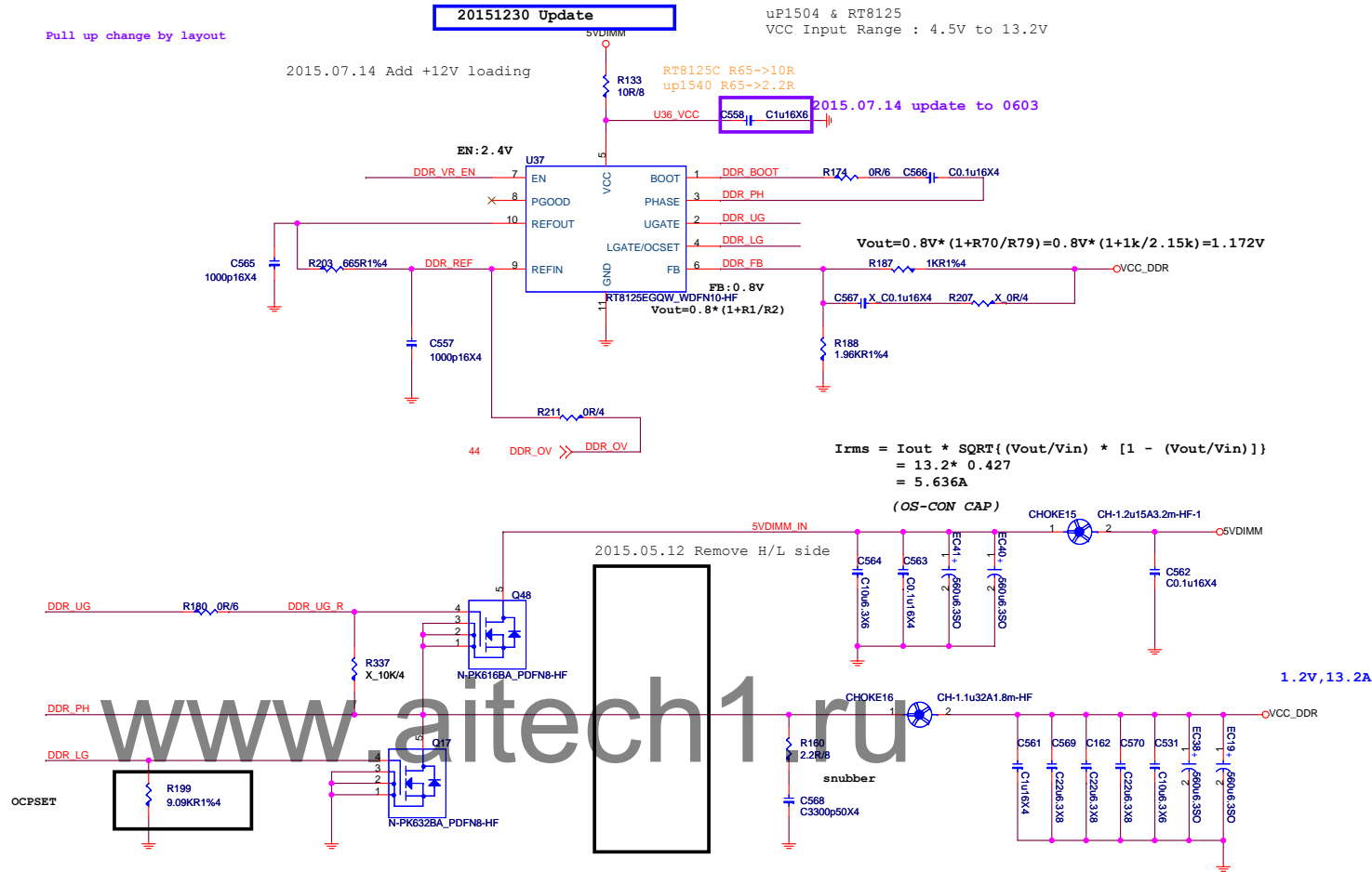




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Size Custom	Document Description VCORE(P-PAK) PHASE1-3	Rev 10
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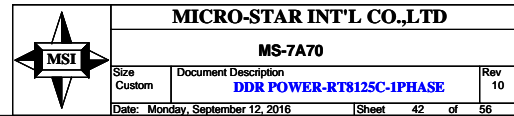
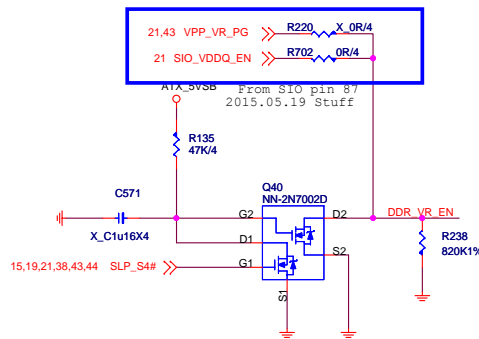


$$\begin{aligned} OCP &= 13.2A * 1.5 = 19.8A \\ R_{ocs}(R95) &= OCP * R_{dson}[Low\ side] / 10uA \\ &= 19.8A * 4.6m\Omega / 10uA \\ &= 9.108K \end{aligned}$$


Datasheet 20A 環衛

$$L_{min} = ((V_{in} - 1.2V) / (F_{sw} * k * I_{out\_max})) * (V_{out} / V_{in})$$
$$= 0.7677\mu H \quad (K = 30\%)$$

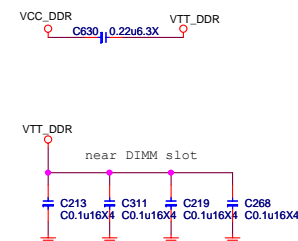
環脒 CAP ESR環脒,  $0.2432\mu\text{H} \leq L \leq 1.2897\mu\text{H}$



OCP=2.24A\*1.5=3.36A????



2.24A



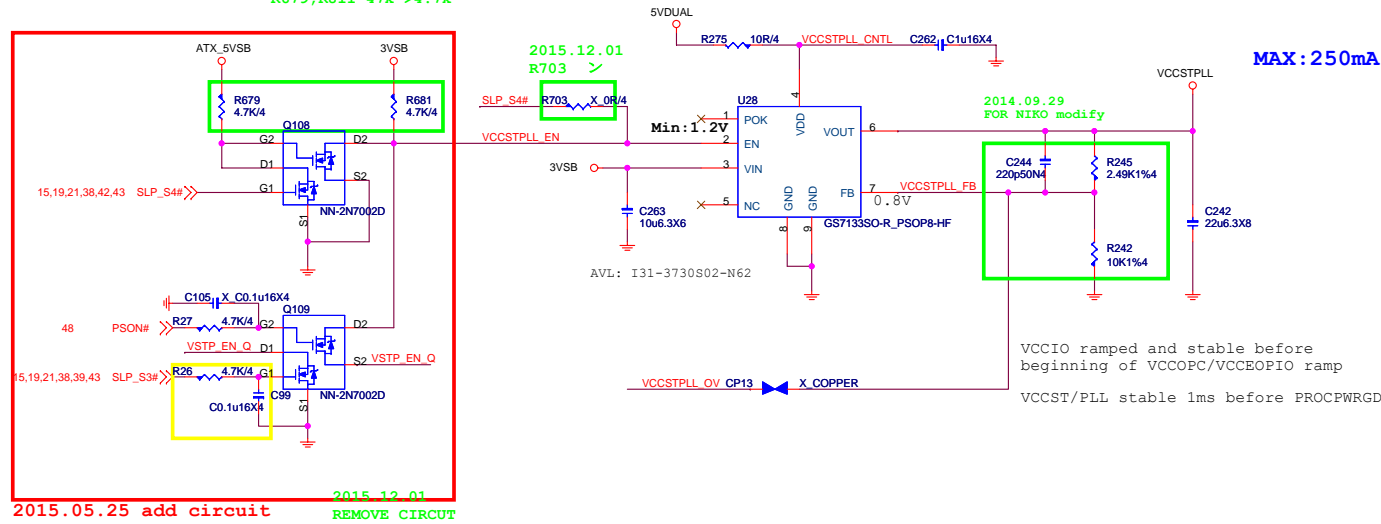
Size Custom	Document Description <b>DDR-MP2147-VPP25</b>	Rev 10
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## VCCSTPLL

1.0V; 250mA

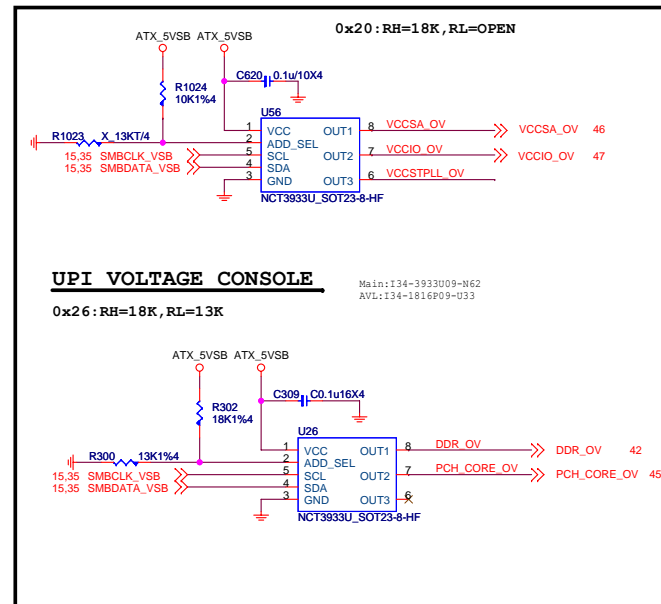
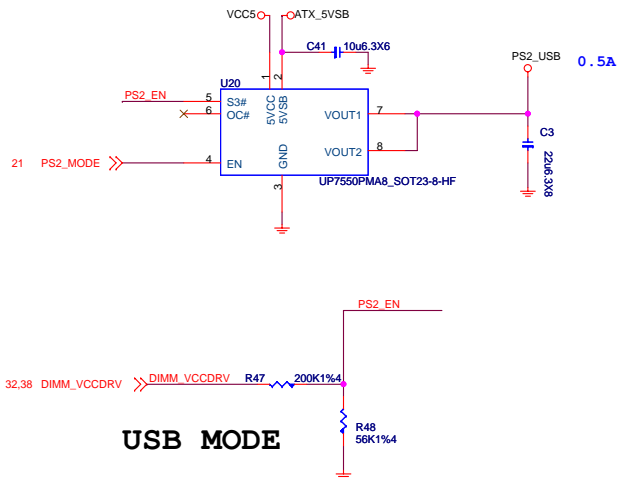
For Cost down VCCST&VCCPLL merge

2015.12.01  
R679,R811 47k->4.7k



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## PS2 POWER



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# PCH 1VSB

1.0V; 11A

OCF = 11A\*1.5=16.5A

Rocset = 1.5 \* Imax \* Rdson(low) / Iocset  
= 1.5 \* 11A \* 4.6mohm / 10uA  
= 7.59K

Rdson(low) 4.5V

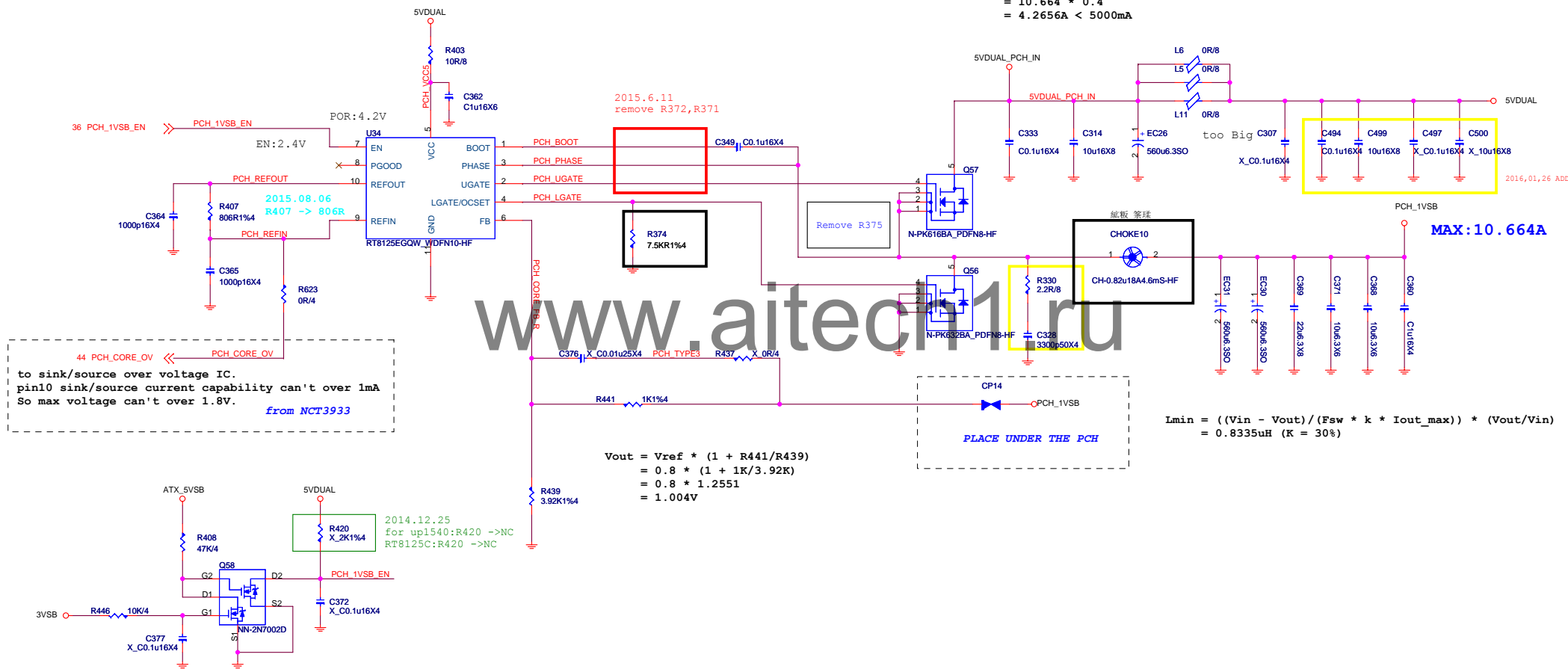
D03-4C05N03-005 : 5 mohm  
D03-632BA0C-N03 : 4.6mohm  
D03-3056M00-U47 : 6.2mohm

2015.04.23 change to UP1540

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$



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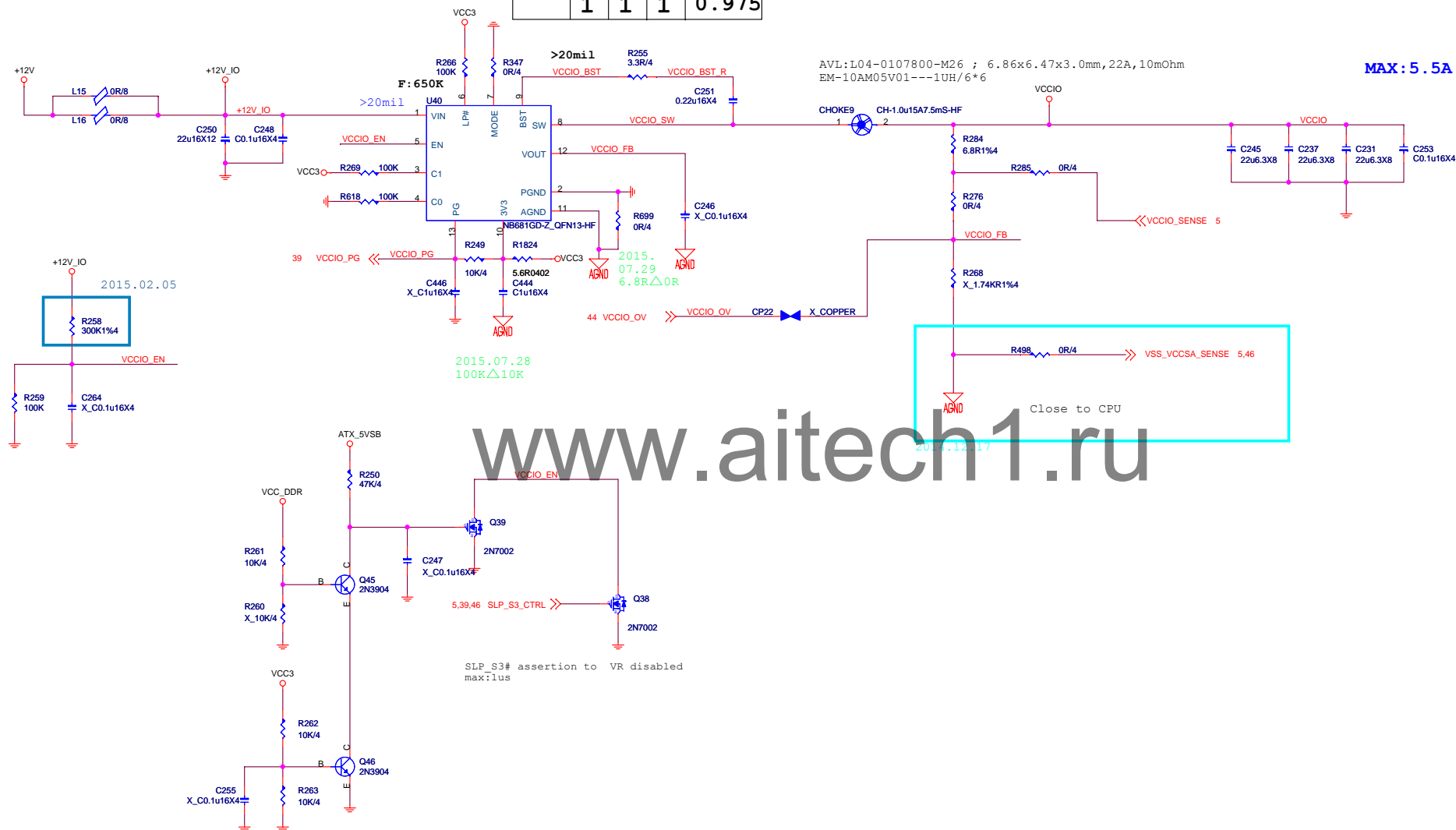
Size	Document Description	Rev
Custom	PCH Core power	10
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# VCCIO

IMAX 6A  
0.95V; 5.5A  
ILIMIT=8.5~9A  
OCP=5.5A\*1.5=8.25A

LP#	C1	C0	VOUT (V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975





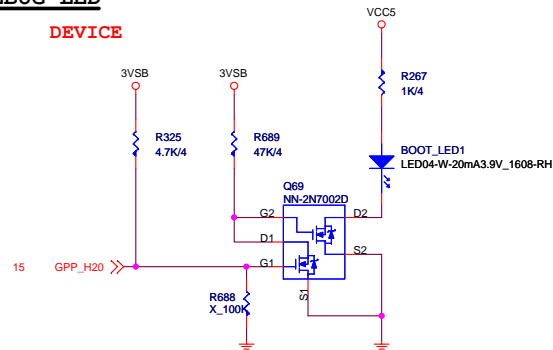
---



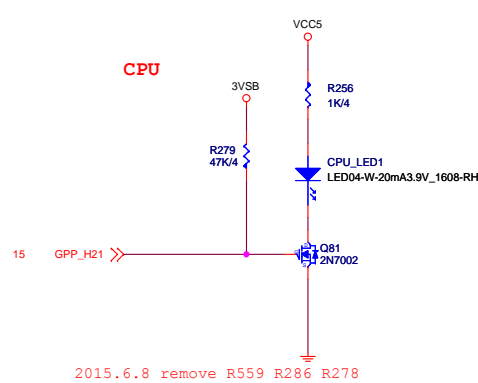


## DEBUG\_LED

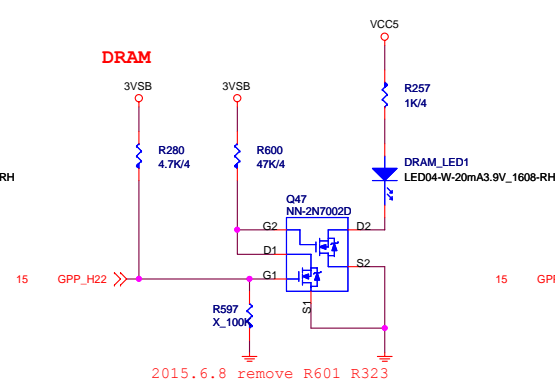
### DEVICE



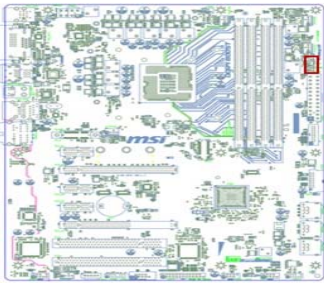
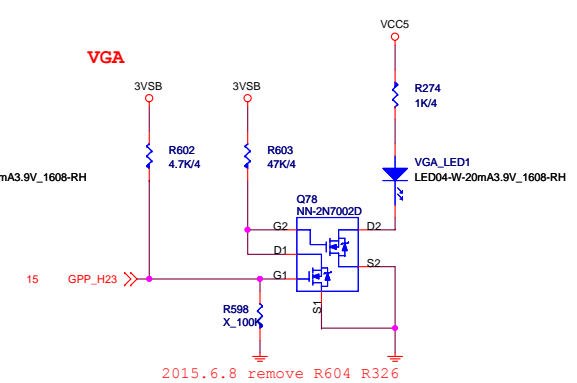
### CPU



### DRAM

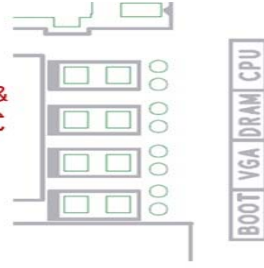


### VGA



EZ Debug  
必須需位於  
JPWR1上方

LED 方向 &  
文字面樣式



## LED

: DOC-040P100-H91  
AVL: DOC-040S500-E07

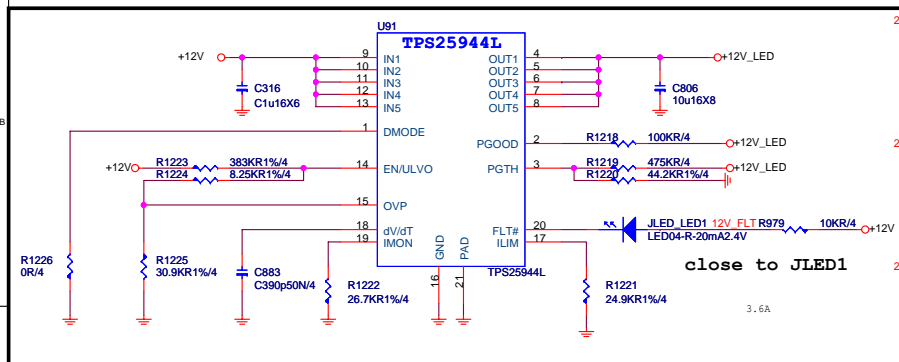
## LED

7 : DOC-040T200-H91  
AVL: DOC-040S200-E07

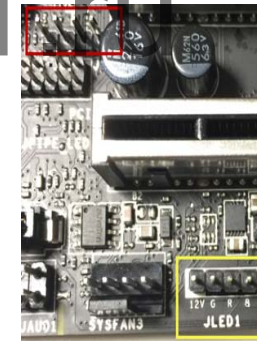
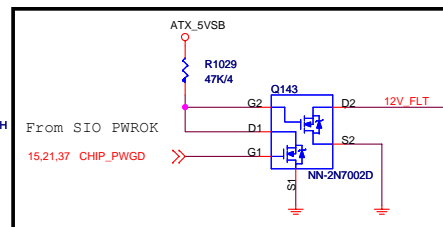
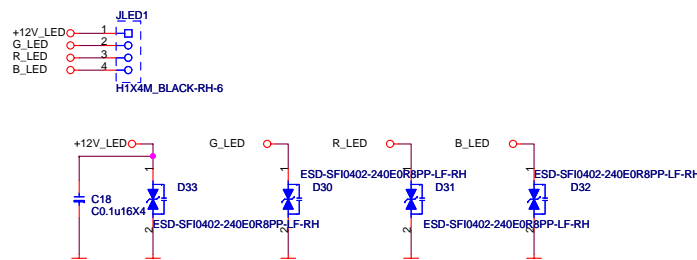
GPIO LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
獠	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

## RGB LED Connector

2016.07.06 Use TPS25941L

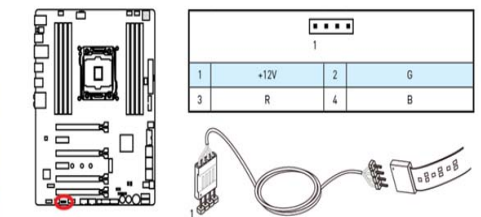


### N31-1040321-P05



## JLED1: RGB LED connector

This connector allows you to connect the RGB LED strip.



## Important

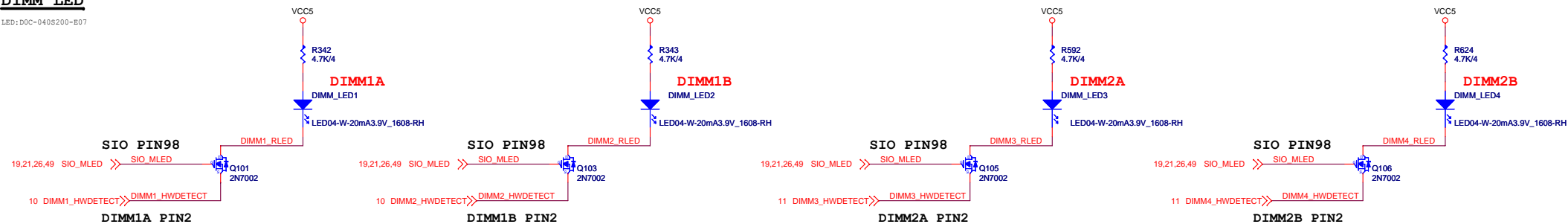
- This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.
- Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.
- Please use the LED Effect of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.



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Custom	DEBUG_LED&RGB_LED Connector	10	
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## DIMM LED

LED: DOC-040S200-E07



## LED

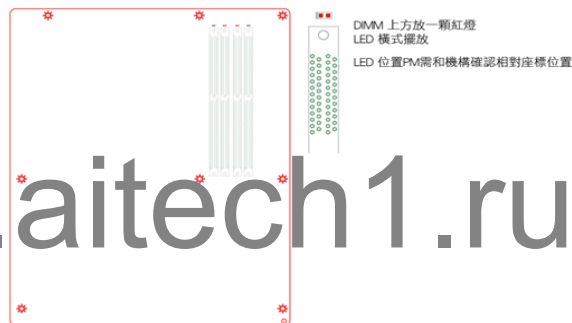
: DOC-040P100-H91  
AVL: DOC-040S500-E07

## LED

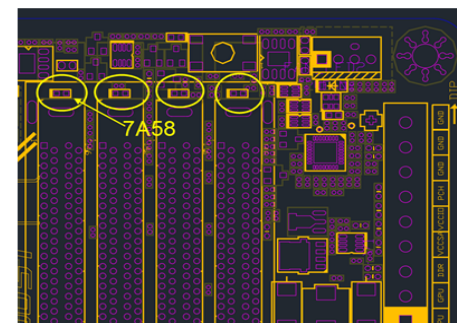
フ : DOC-040T200-H91  
AVL: DOC-040S200-E07

需做紅白LED colay 線路, 因VF值不一樣, 供電的電壓要特別注意.

無上鐵蓋作法 - 參考7A16



上鐵蓋做法 - 參考7A58



## BOTTOM LED

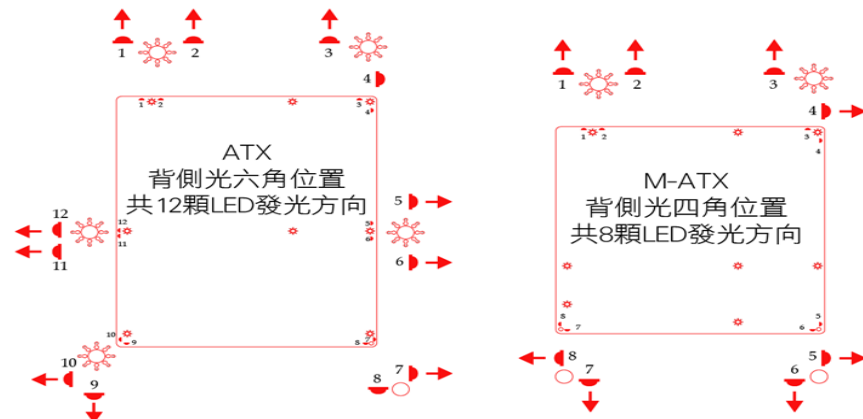
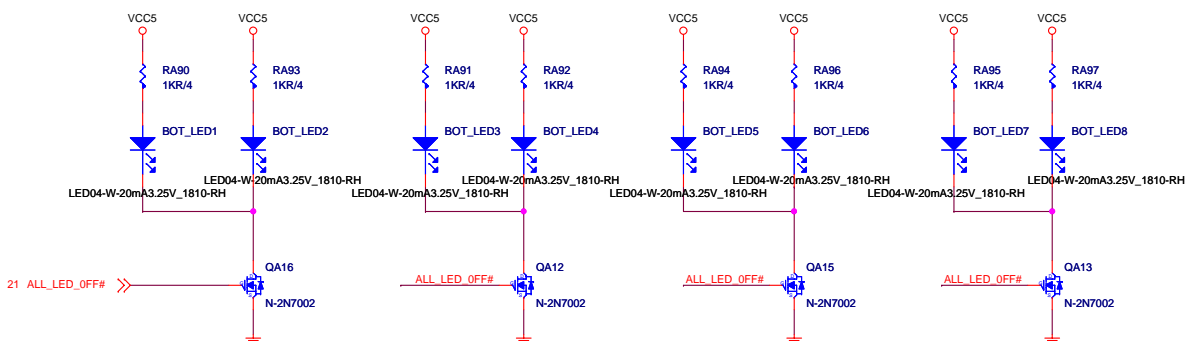
LED: DOC-040S300-E07

## LED

フ : DOC-040T300-H91  
AVL: DOC-040S300-E07

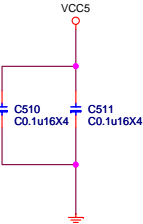
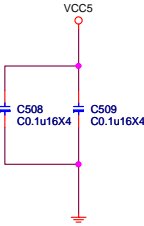
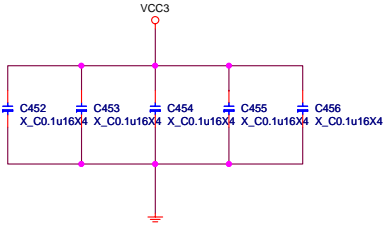
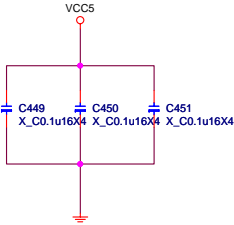
## LED

: DOC-040S600-E07



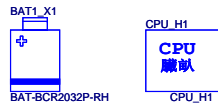
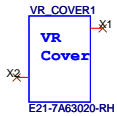
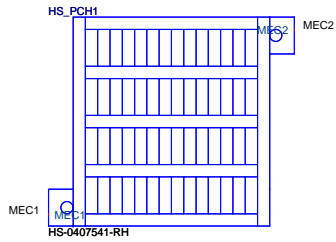
MICRO-STAR INT'L CO.,LTD			
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Custom	DIMM LED&BOTTOM LED	10	
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EMI CAP



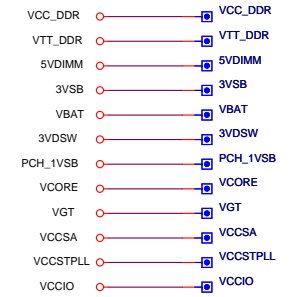
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www.aitech1.ru

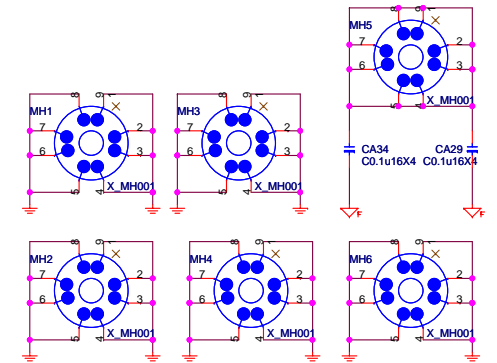


MAIN:PD0-07A7010-G37  
AVL:PD0-07A7010-E48

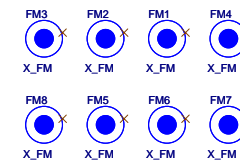
## Test points



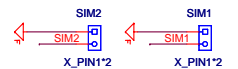
## Mounting Holes



## Optical Fiducial Marks-120



## Simulation



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